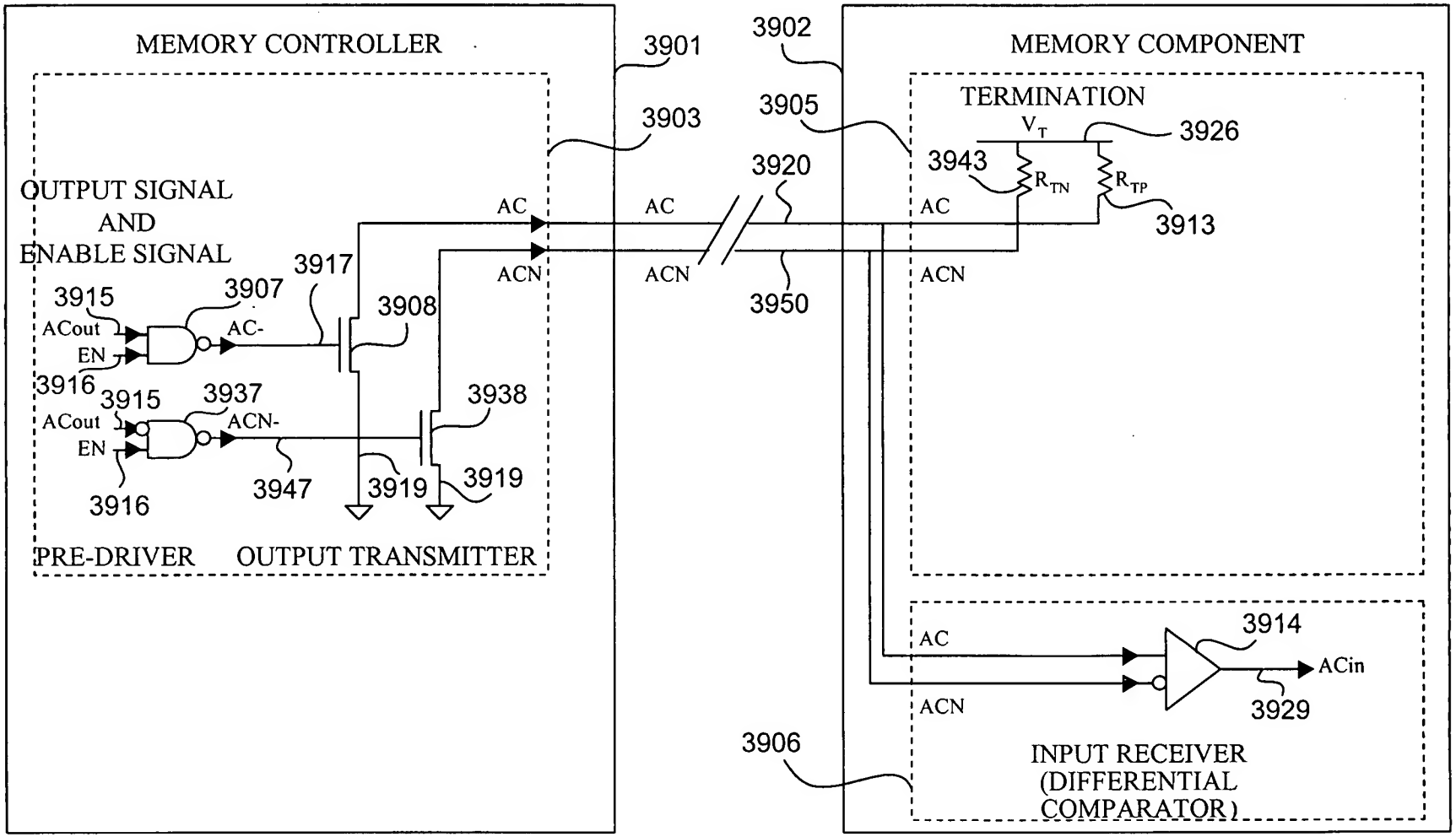


FIG. 39

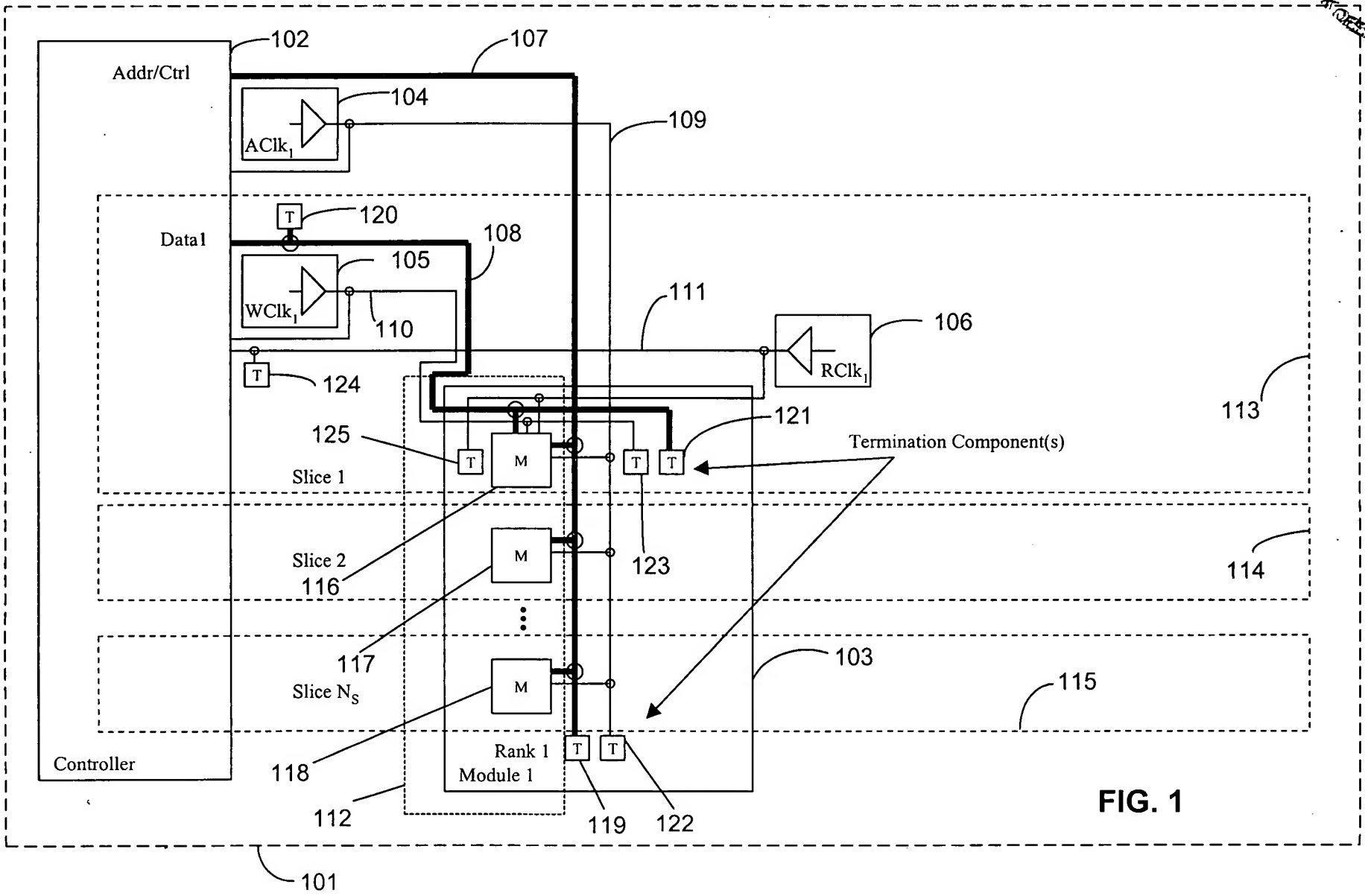


FIG. 1

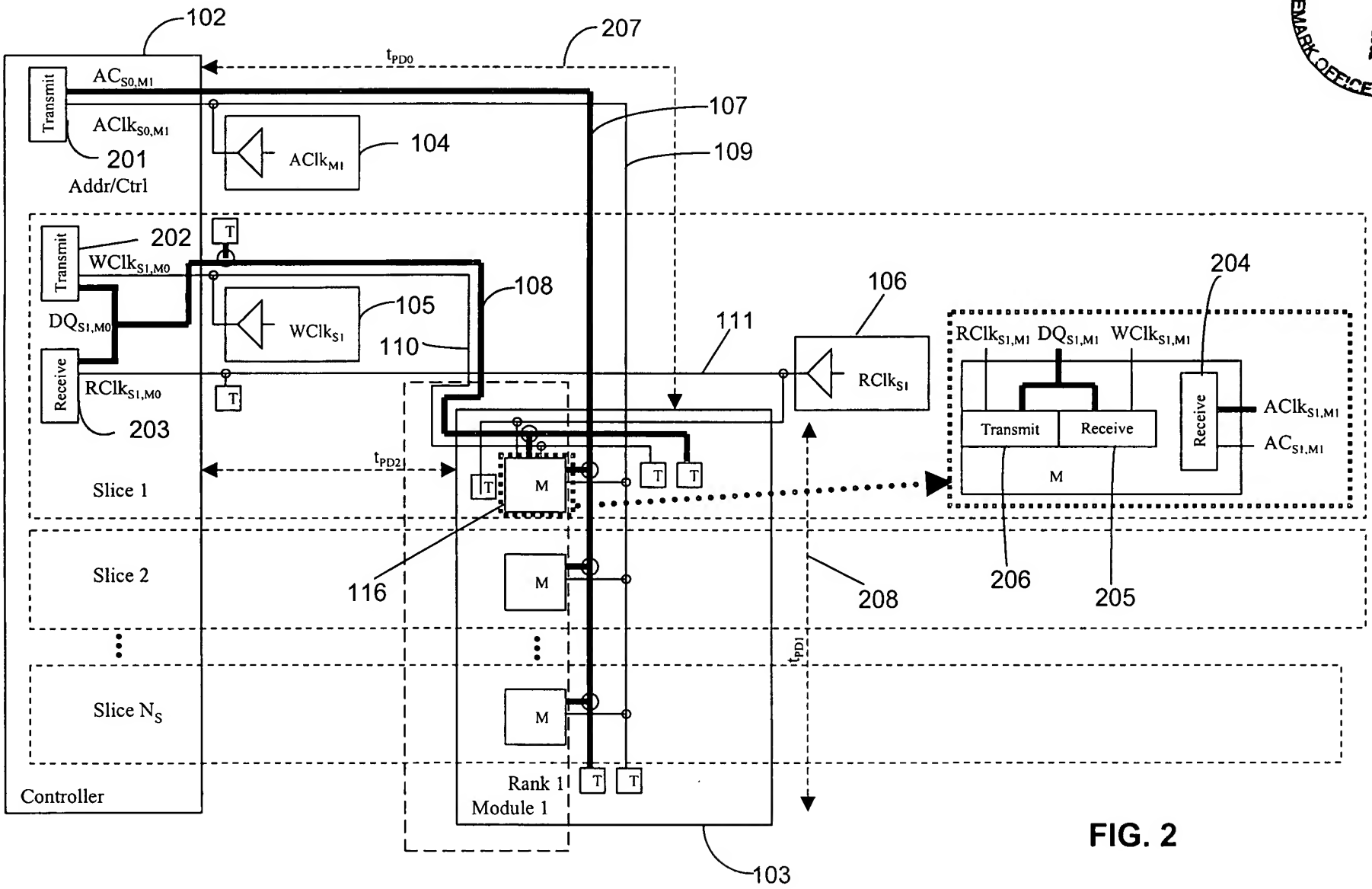


FIG. 2

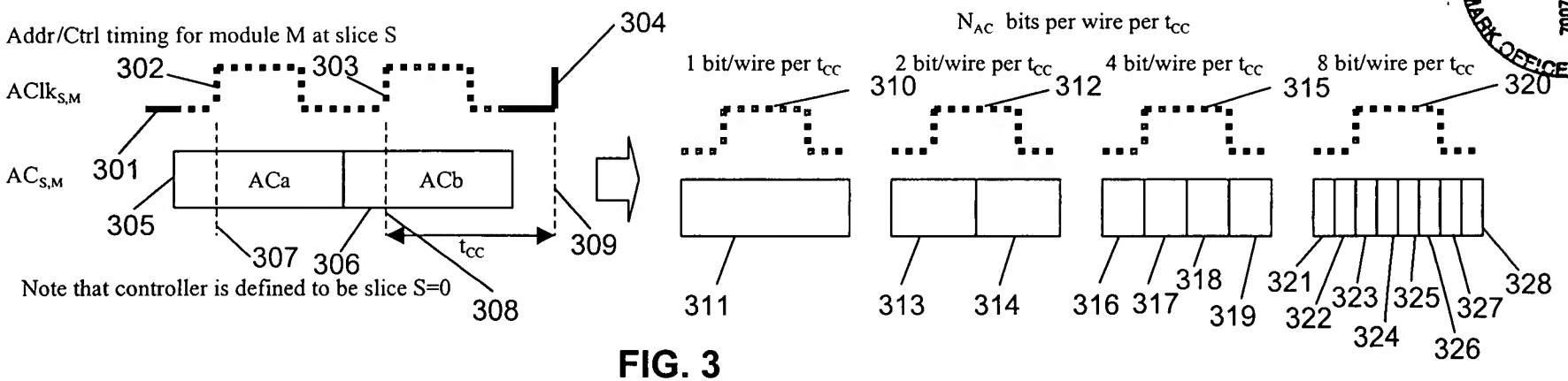


FIG. 3

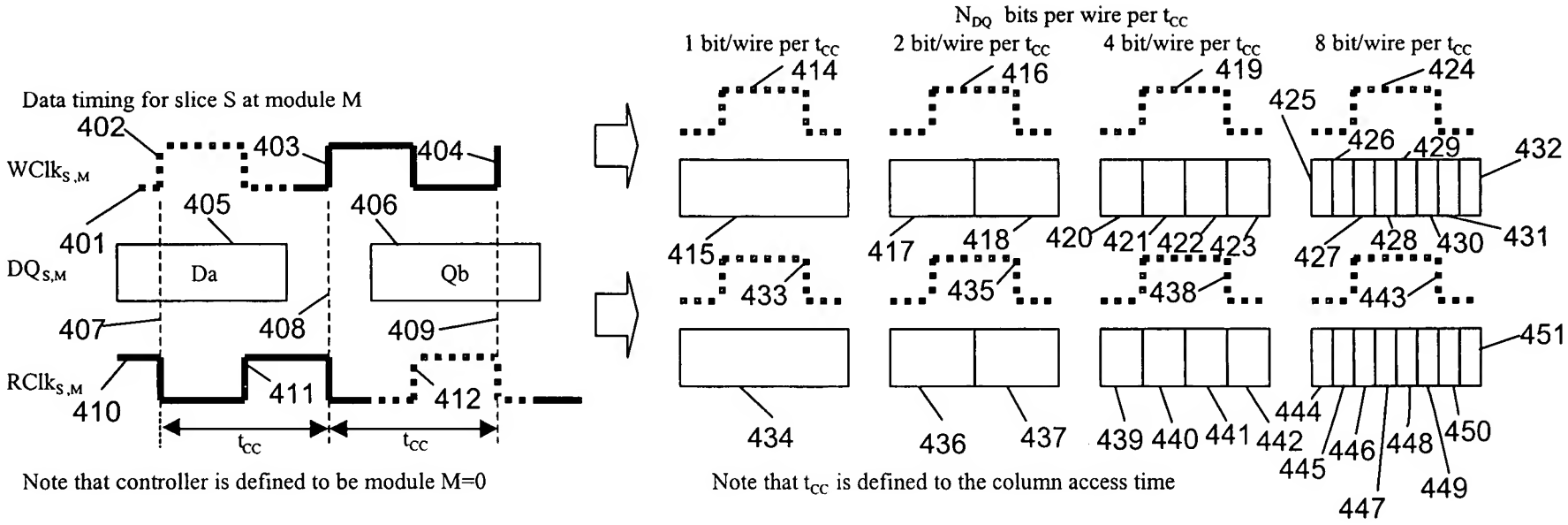


FIG. 4

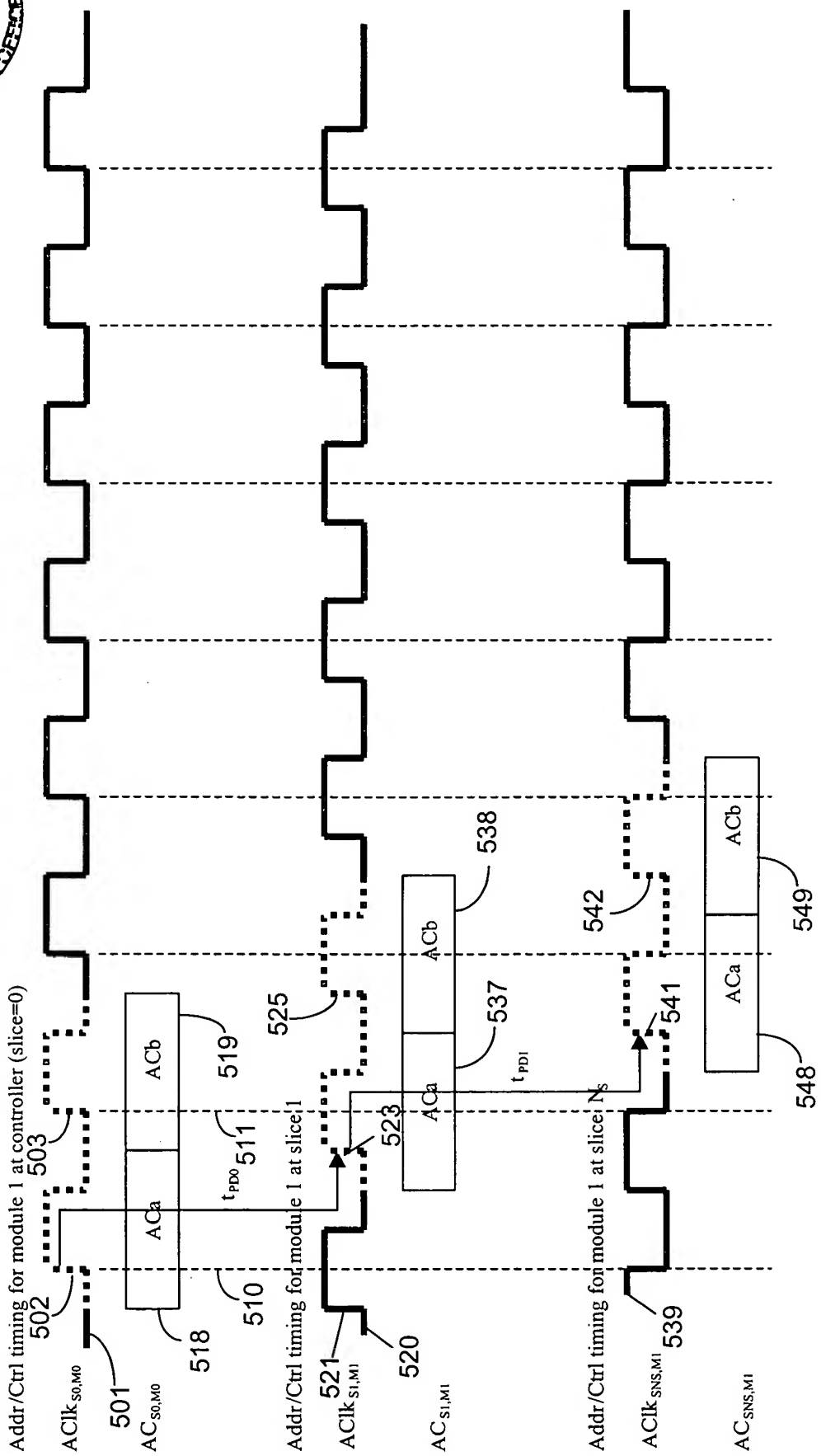


FIG. 5

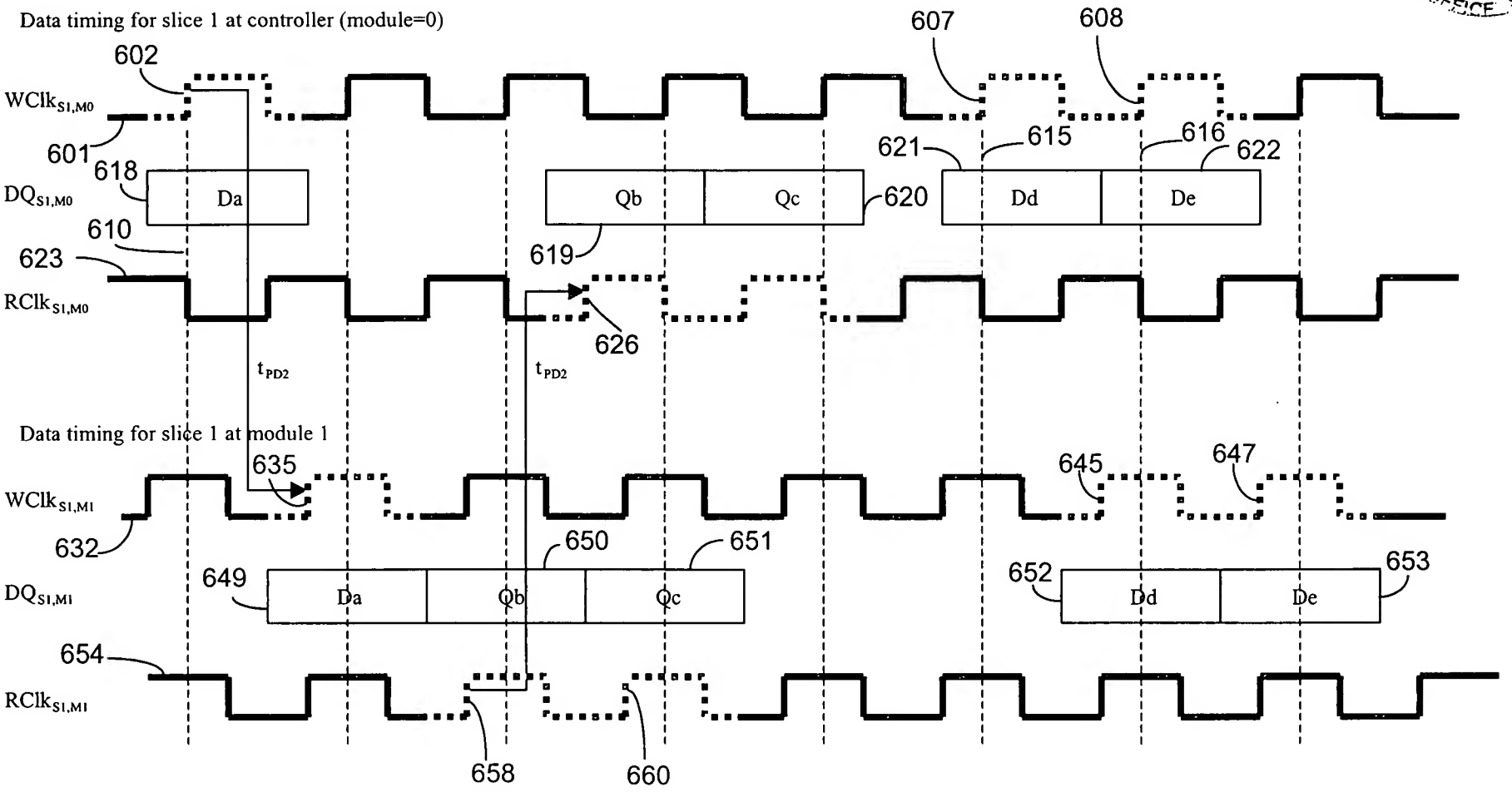


FIG. 6

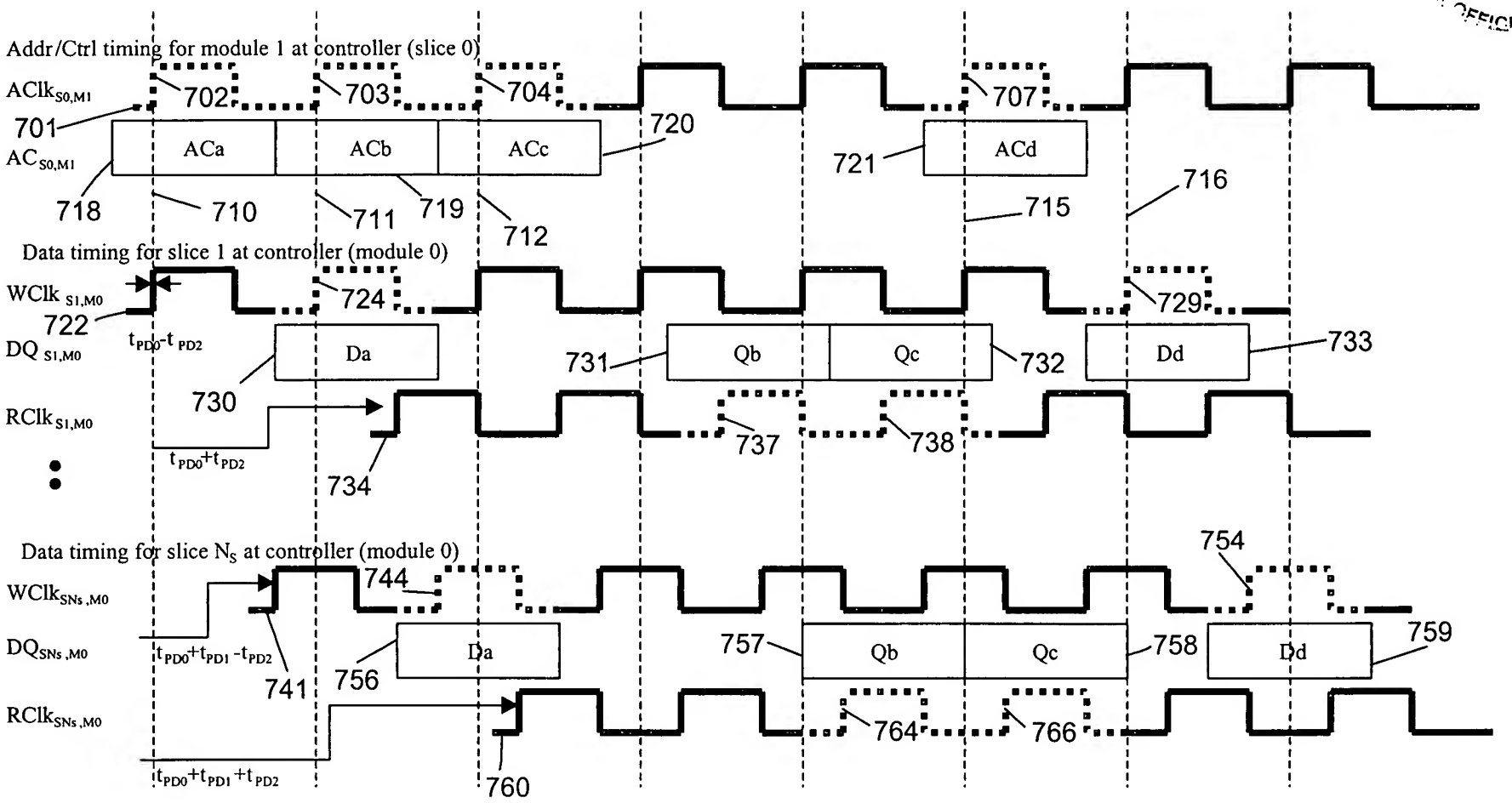


FIG. 7

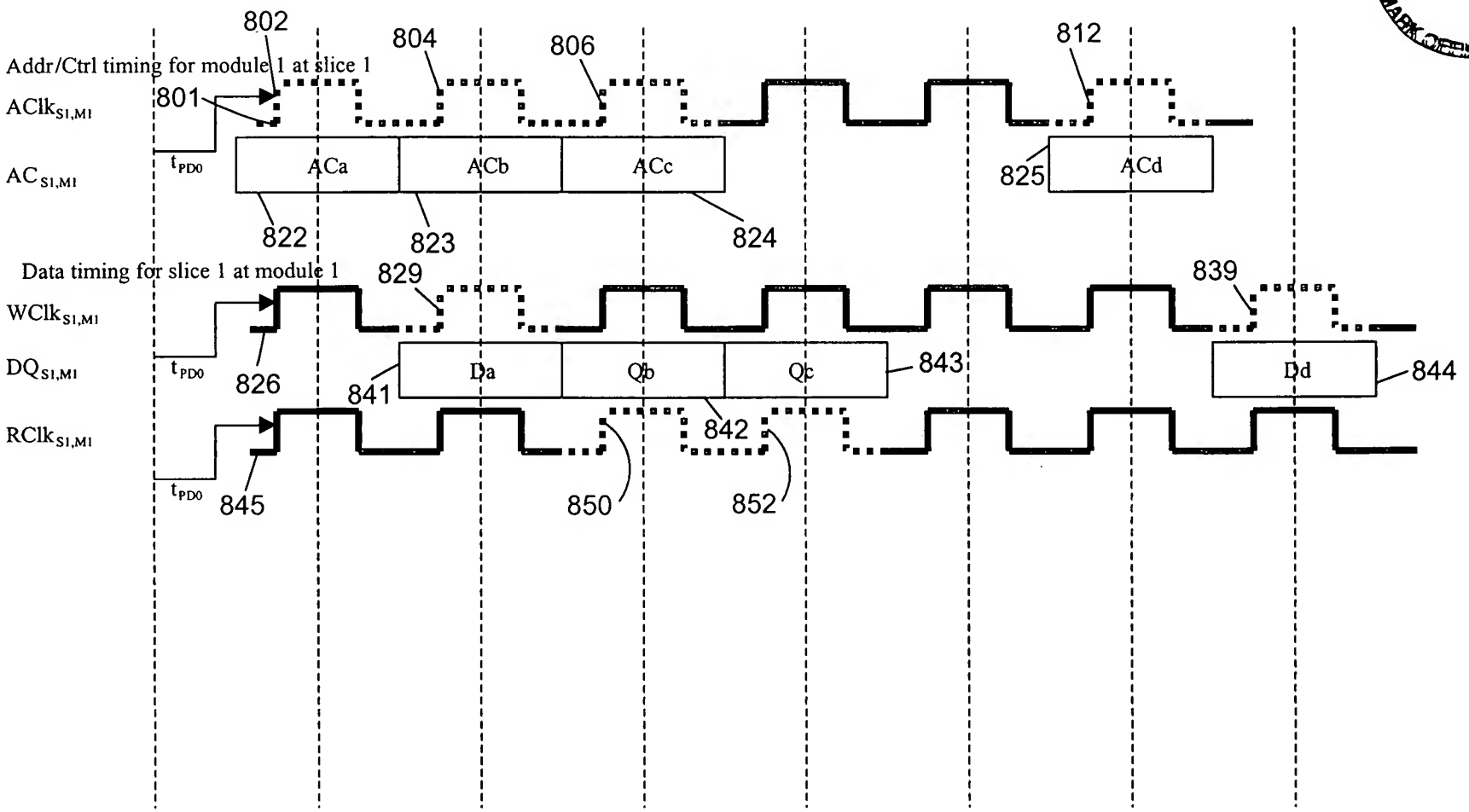


FIG. 8

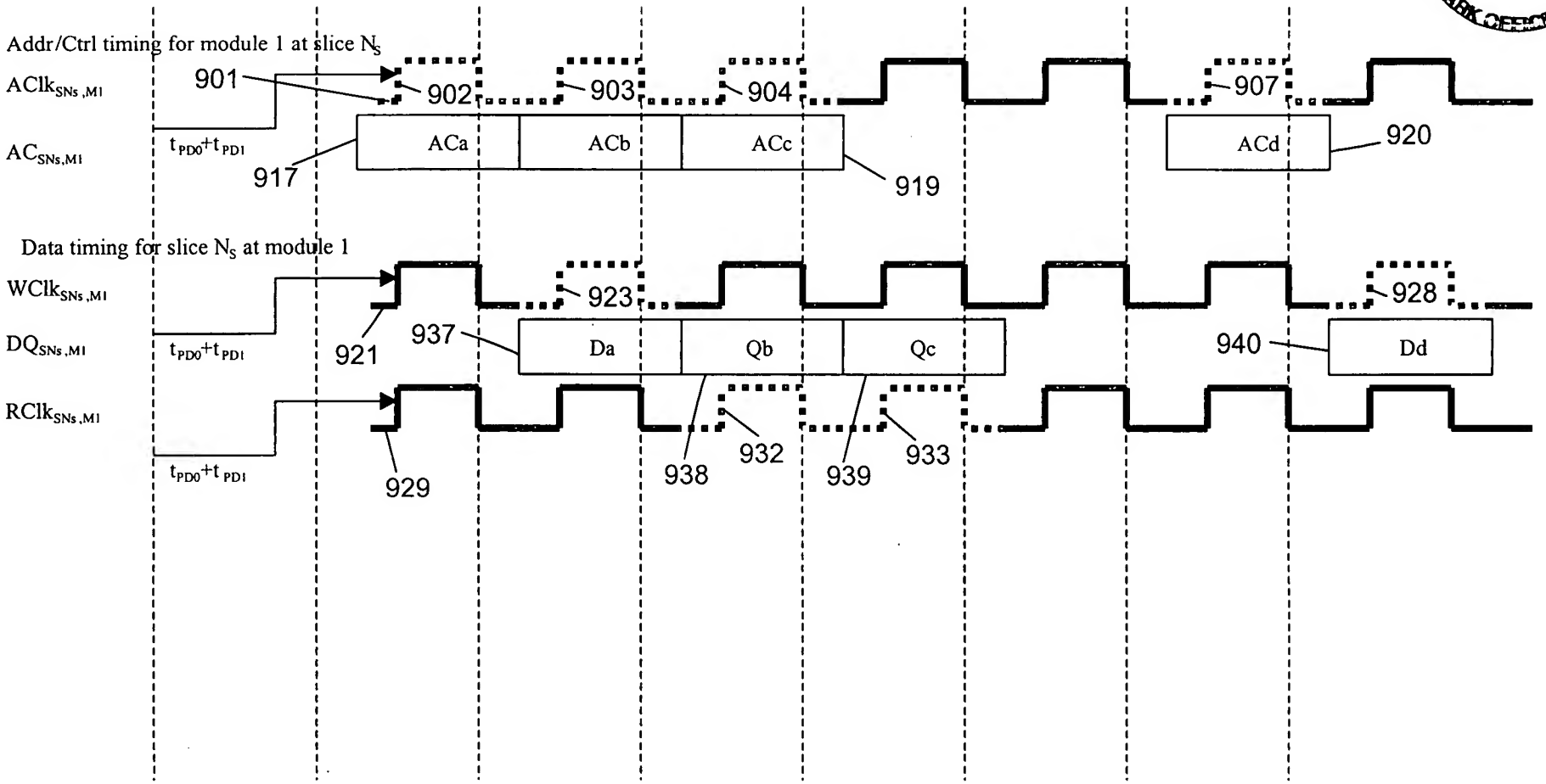


FIG. 9

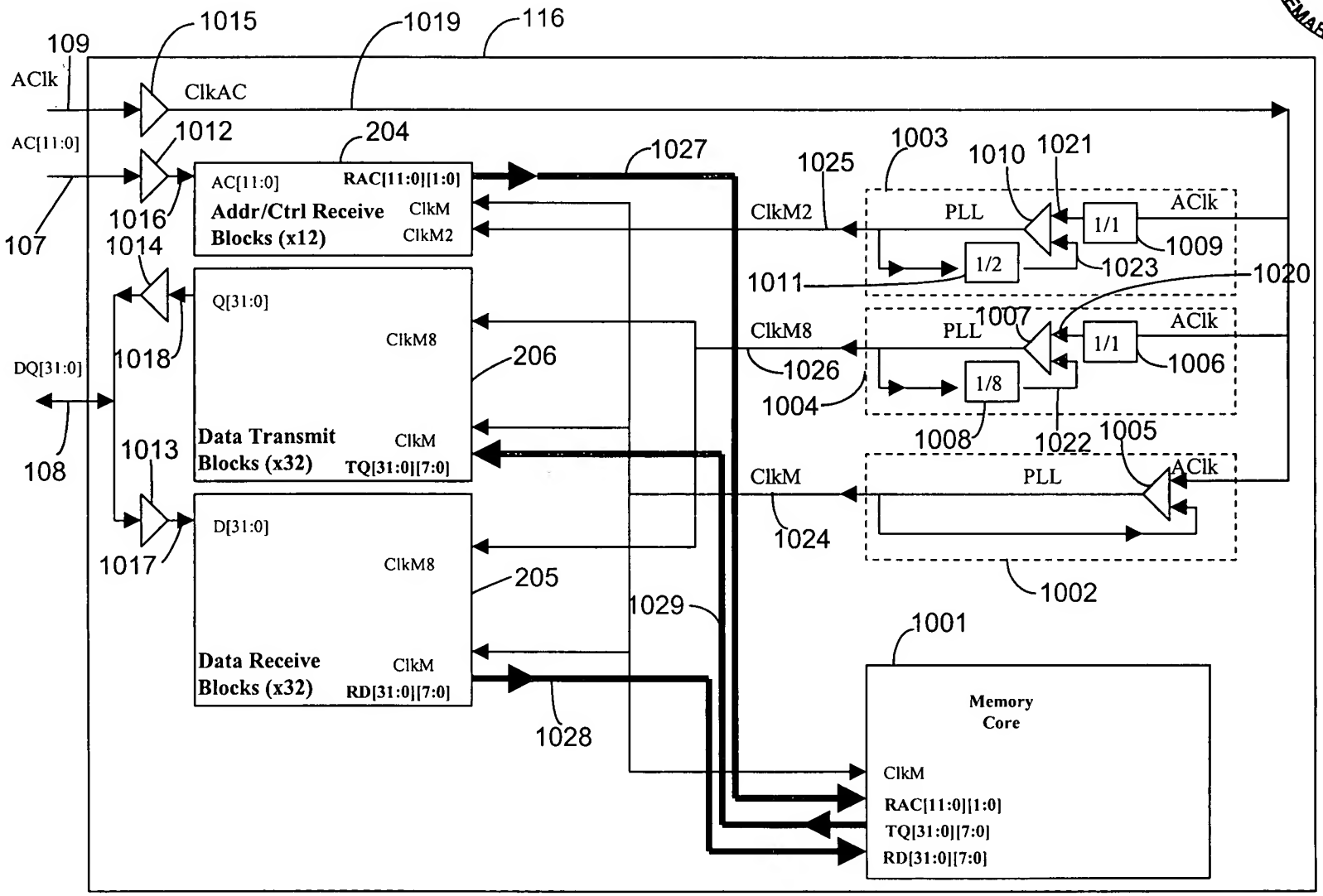


FIG. 10

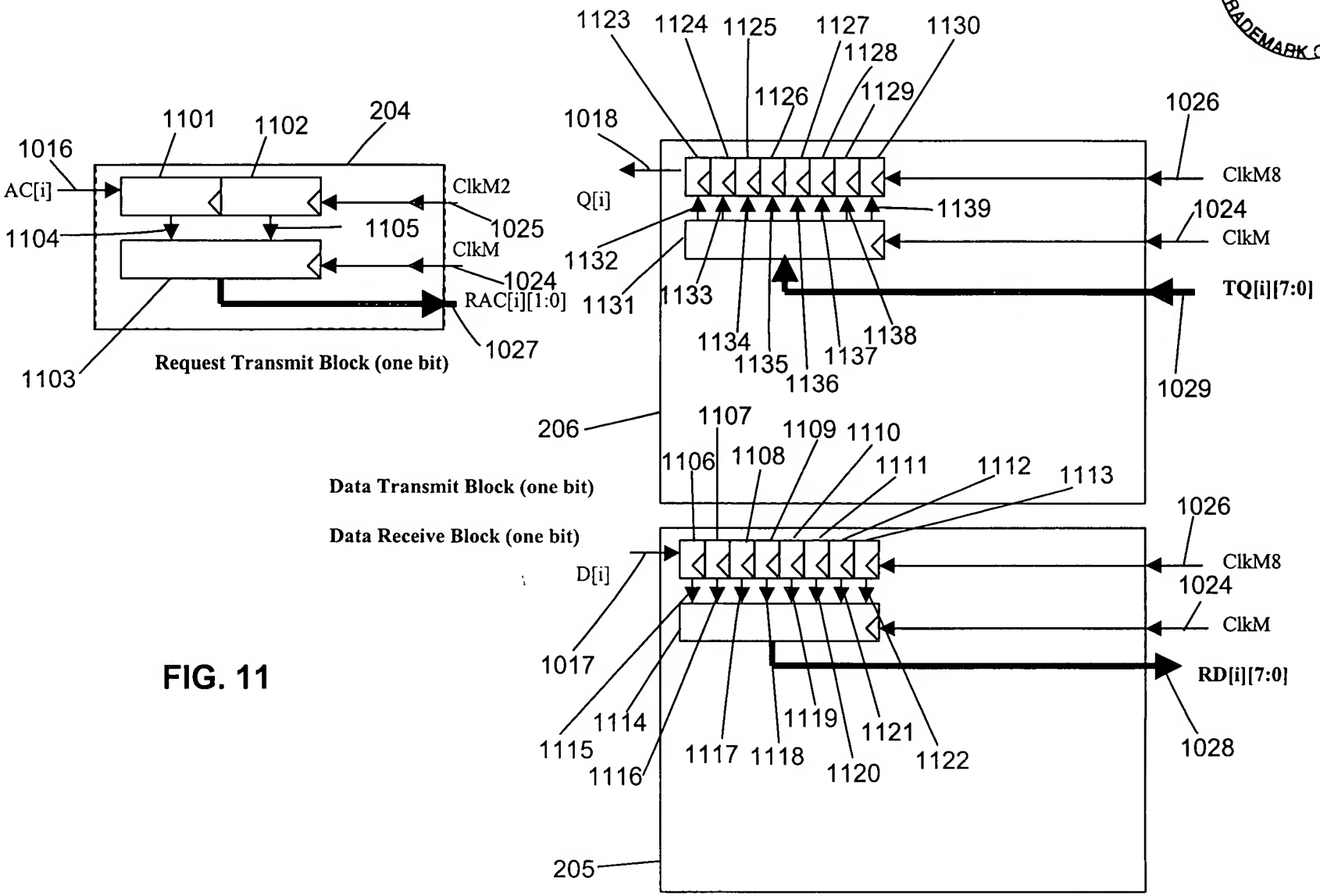


FIG. 11

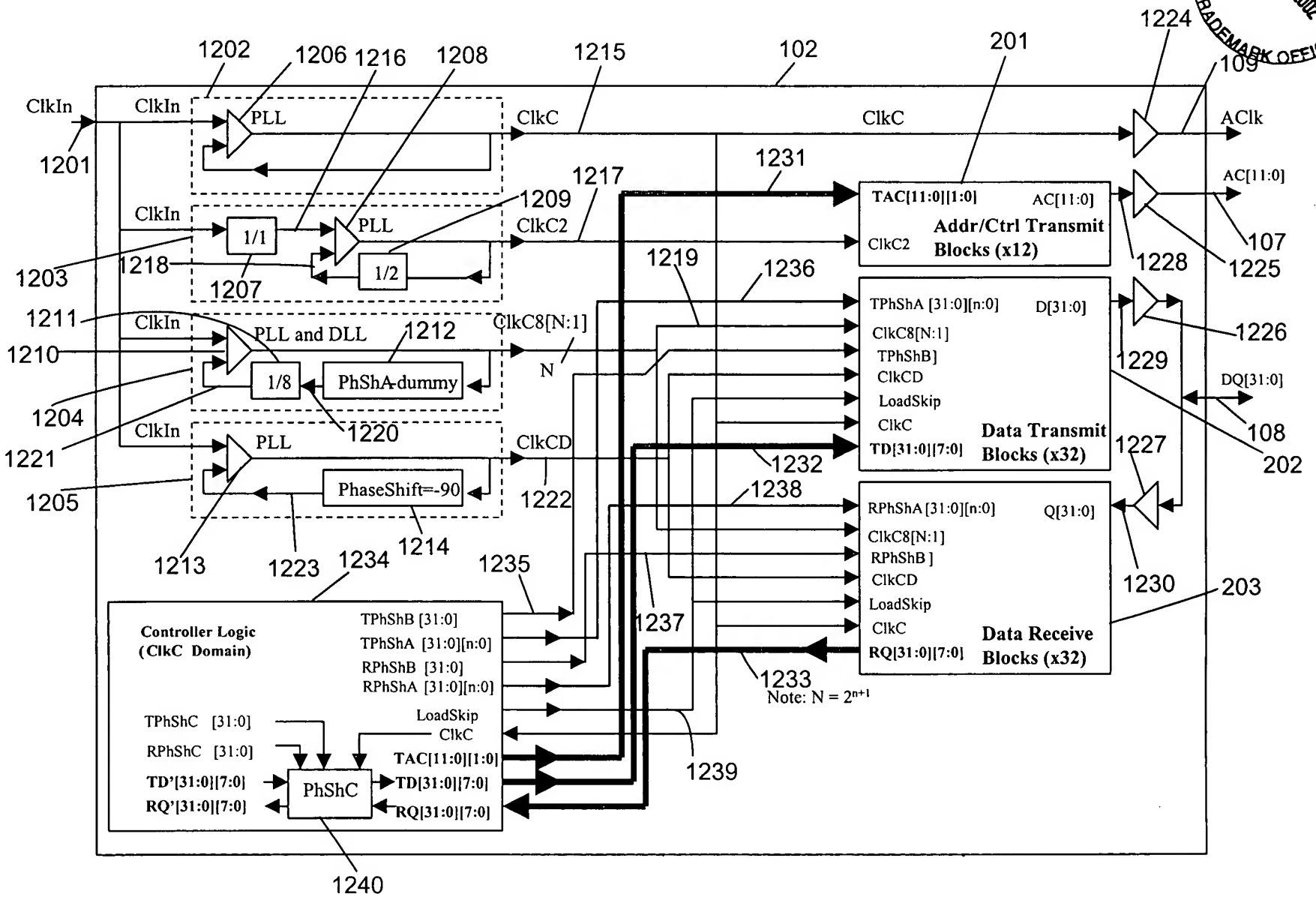


FIG. 12

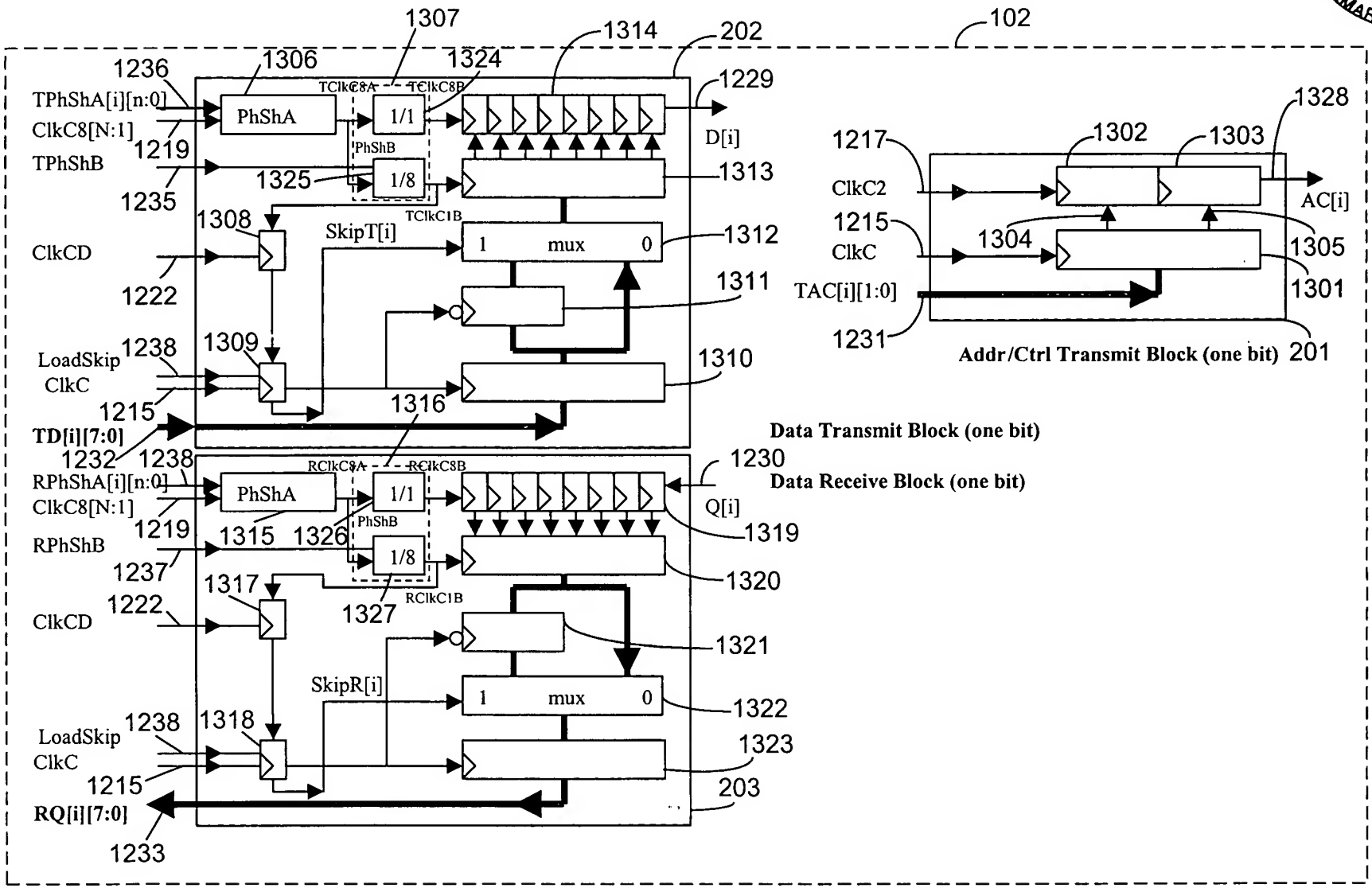


FIG. 13

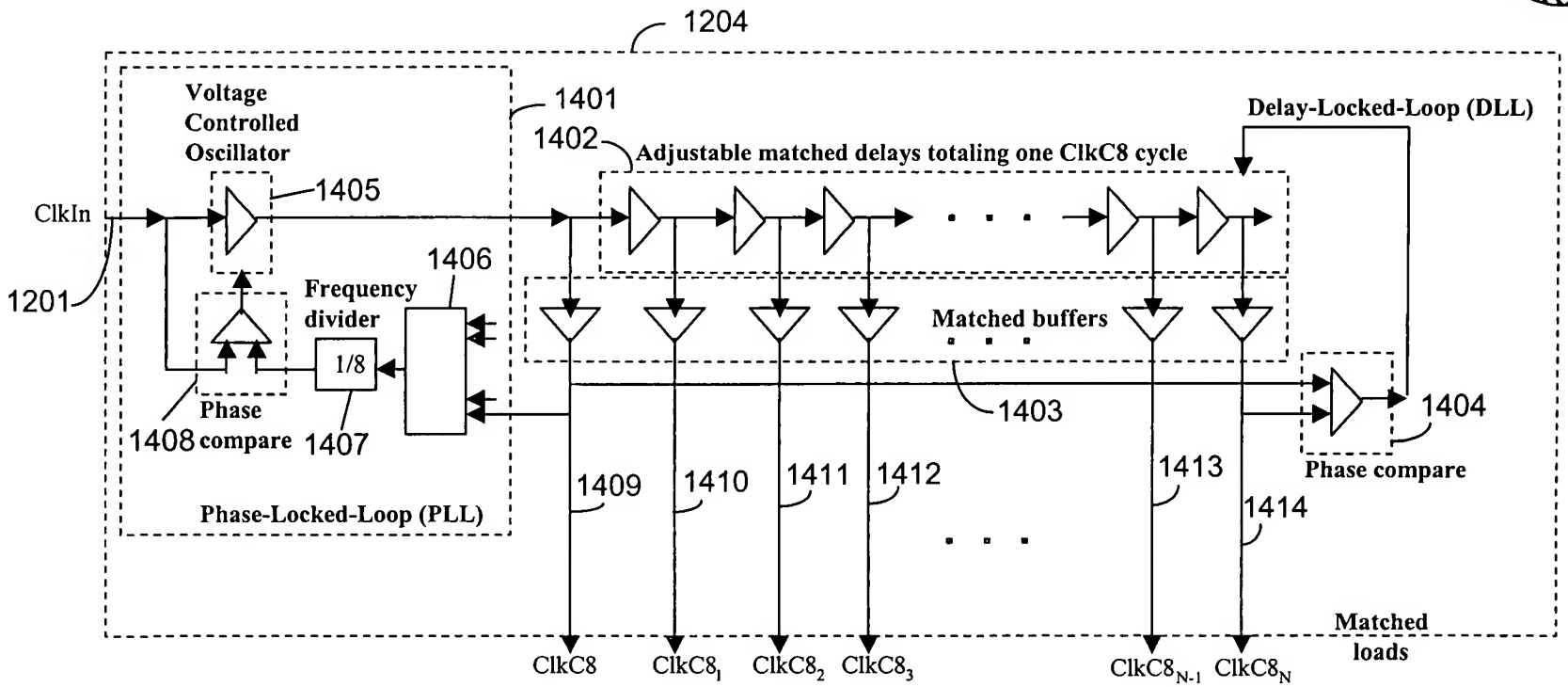
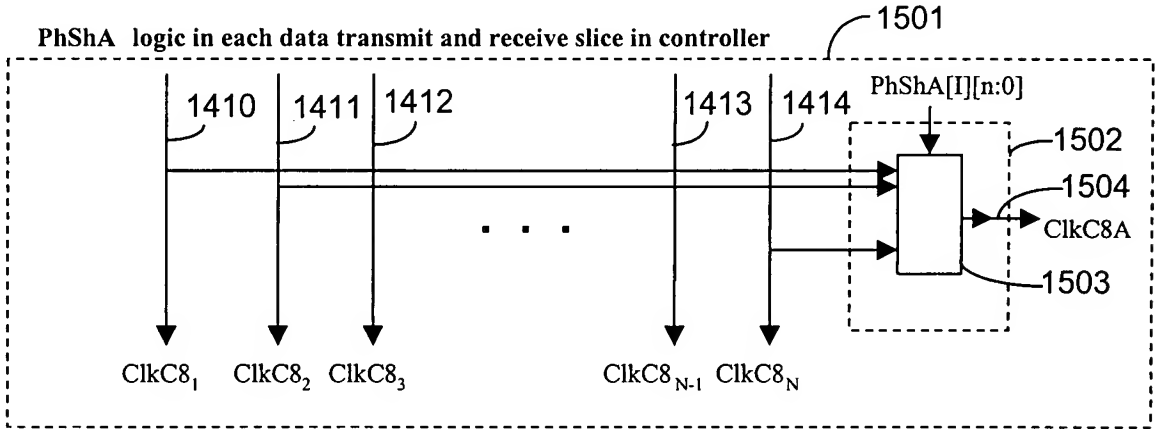


FIG. 14



Note: $N = 2^{n+1}$

FIG. 15

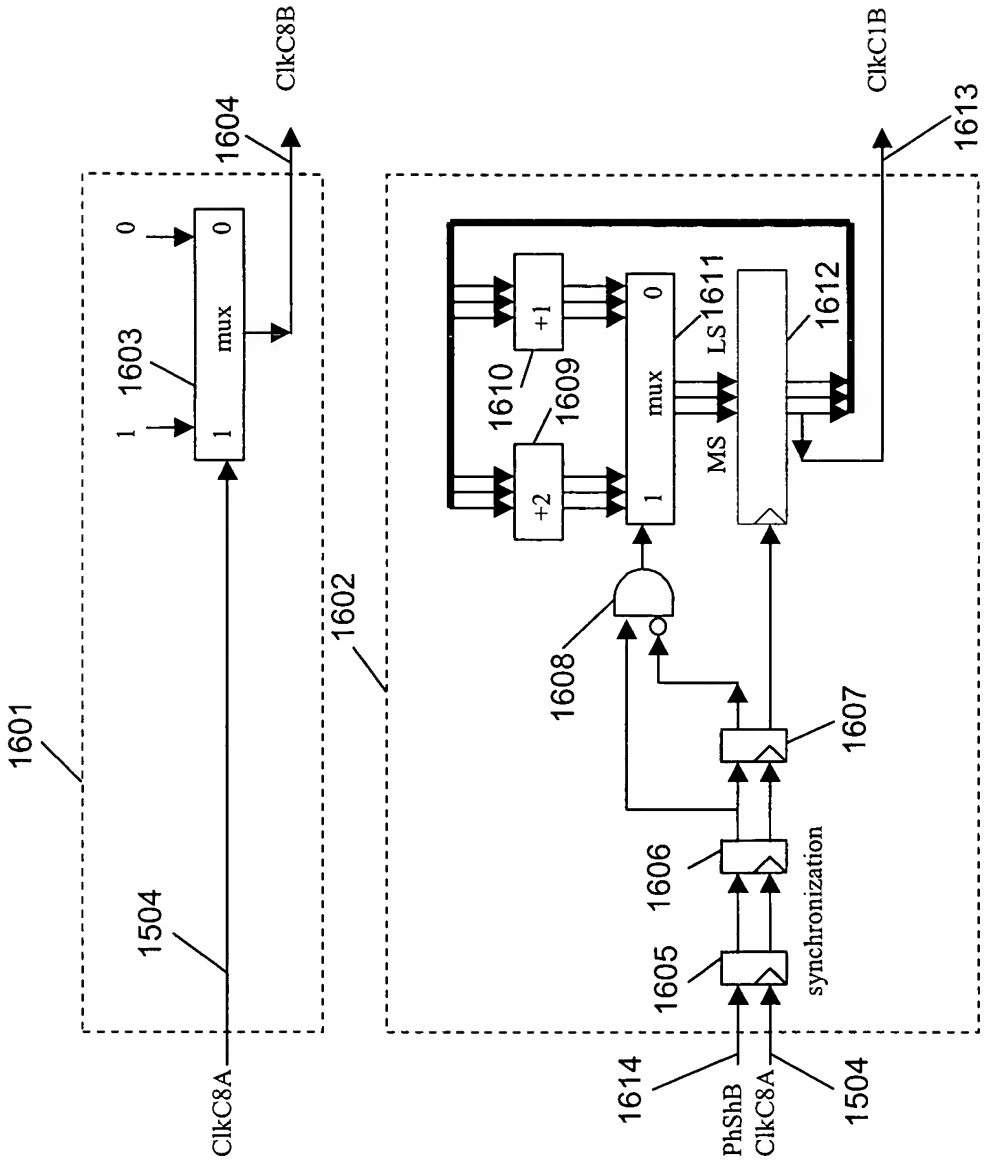


FIG. 16

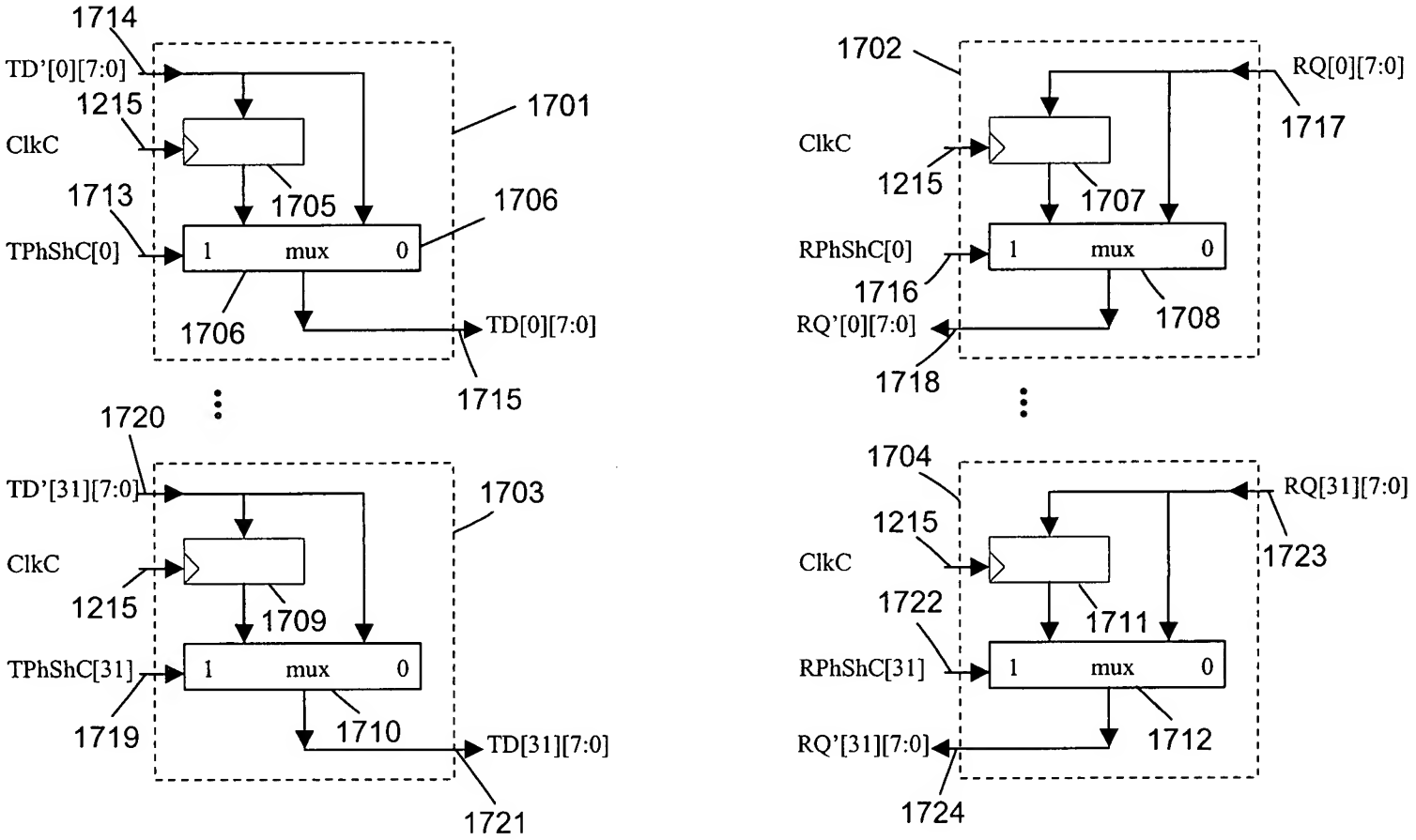

1714
TD'[0][7:0]
1215
ClkC
1713
TPhShC[0]
1705
1706
1
mux
0
1706
TD[0][7:0]
1715
1701
1720
TD'[31][7:0]
ClkC
1215
1709
TPhShC[31]
1719
1710
TD[31][7:0]
1721
1703
1702
RQ[0][7:0]
1717
ClkC
1215
1707
RPhShC[0]
1716
RQ'[0][7:0]
1718
1708
1704
RQ[31][7:0]
1723
ClkC
1215
1722
1711
RPhShC[31]
RQ'[31][7:0]
1724
1712

FIG. 17

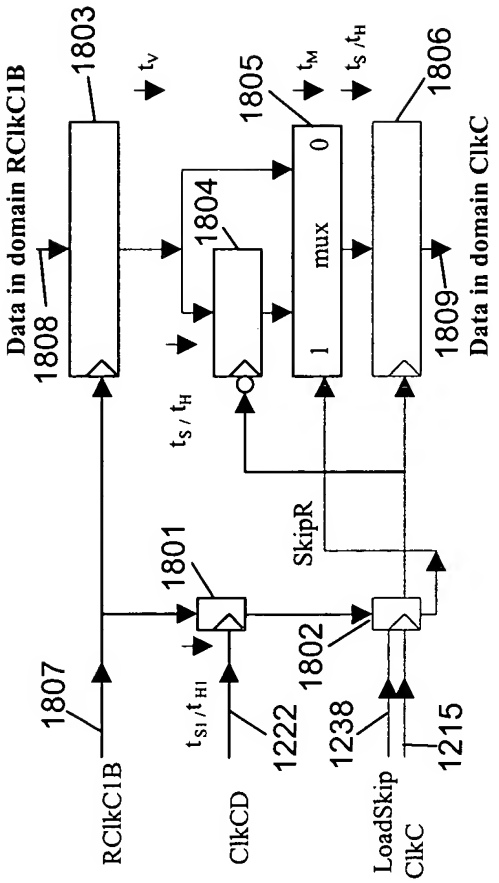


FIG. 18

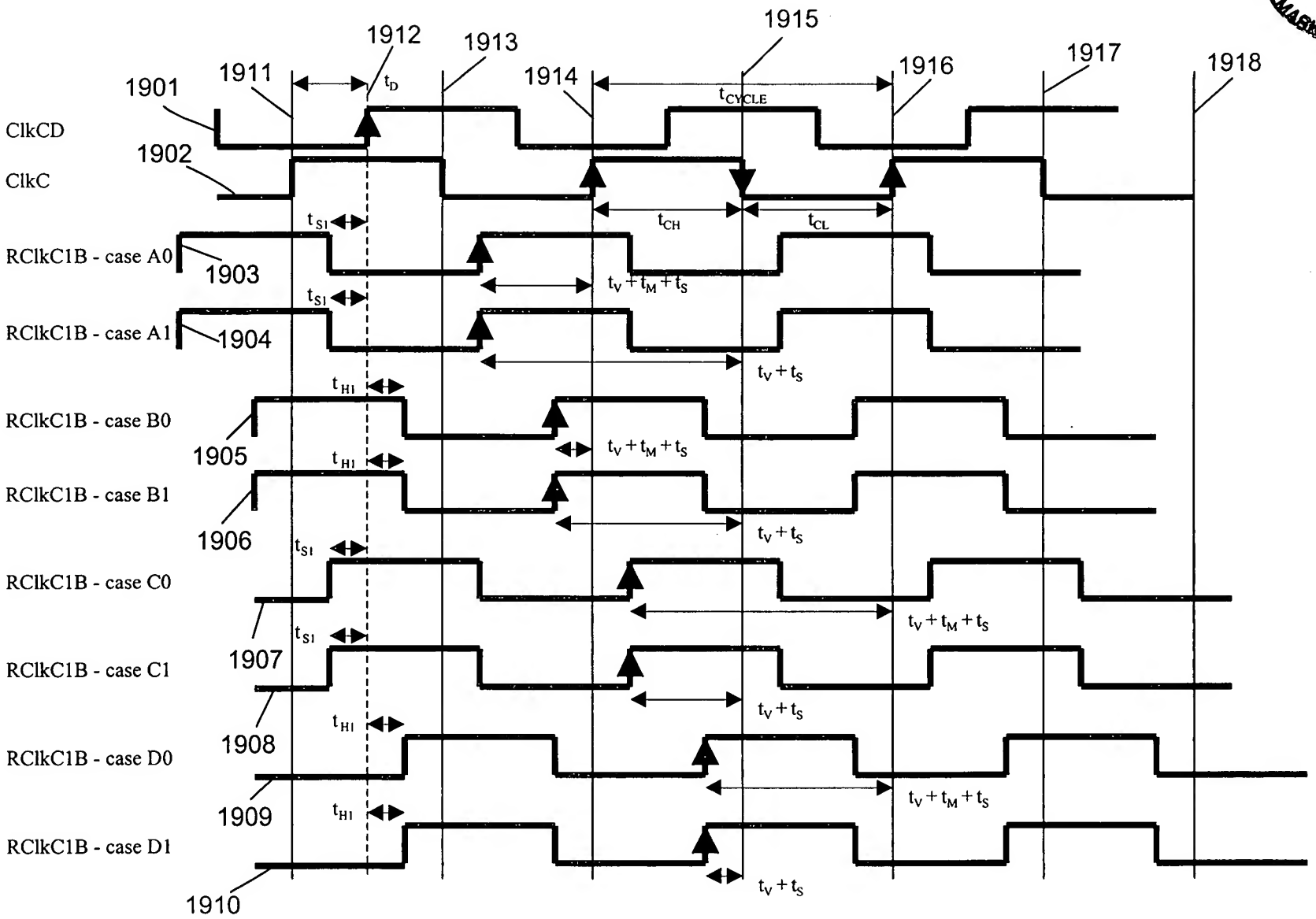


FIG. 19

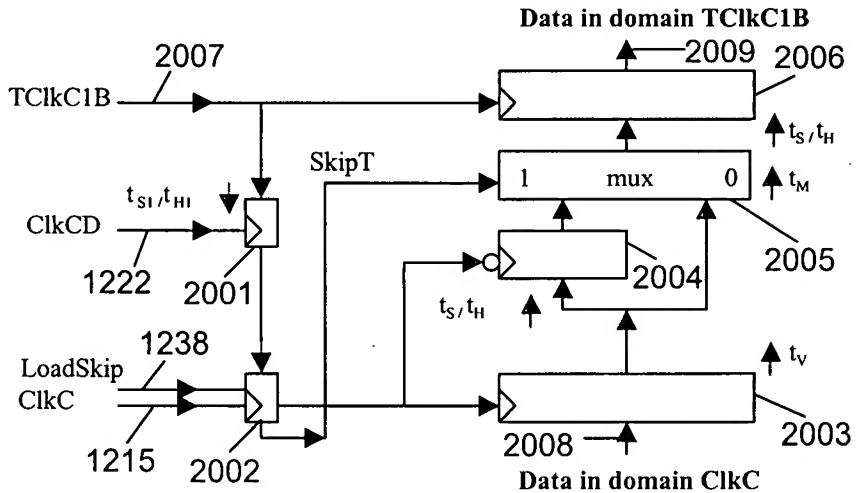


FIG. 20

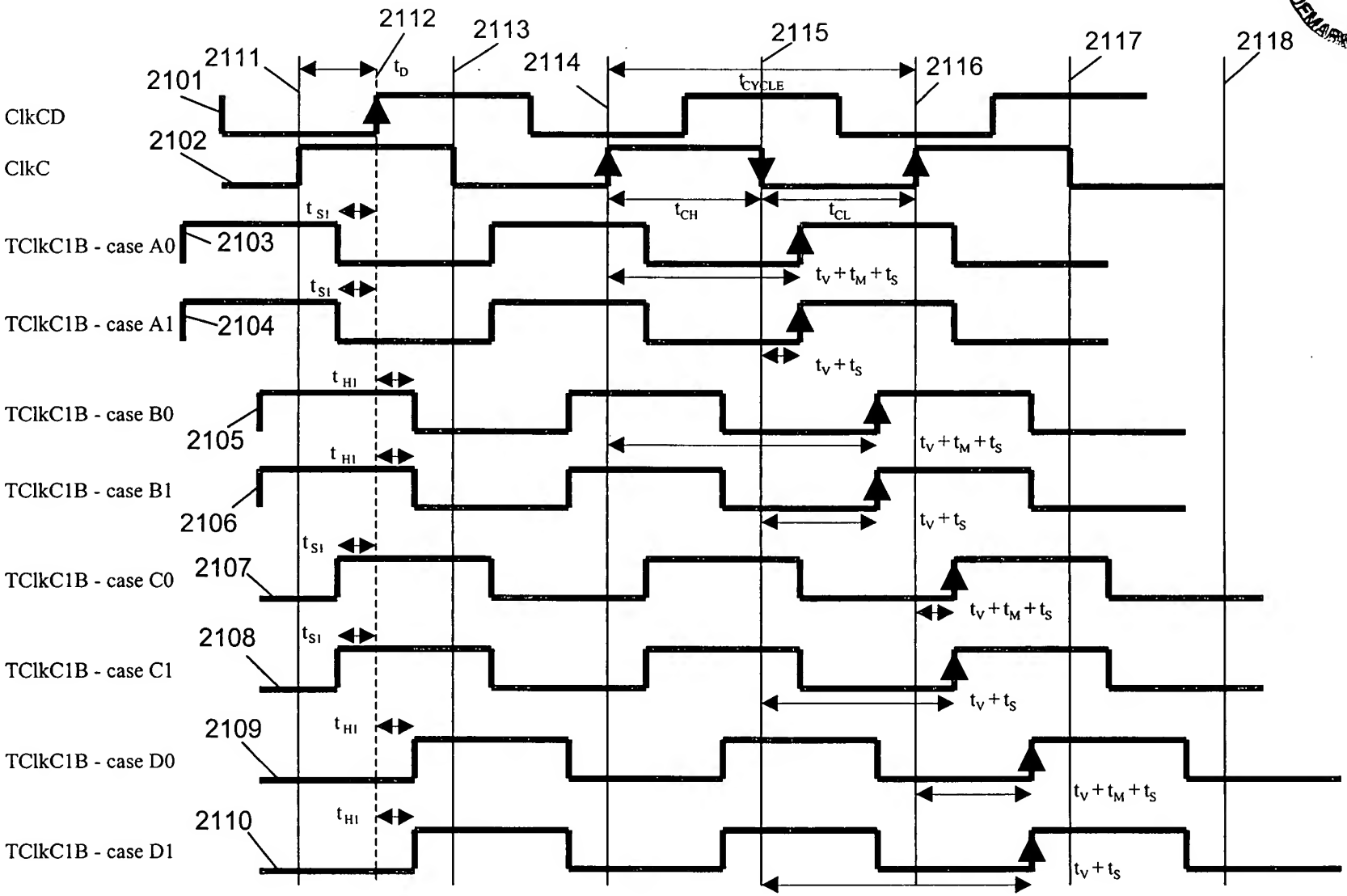


FIG. 21

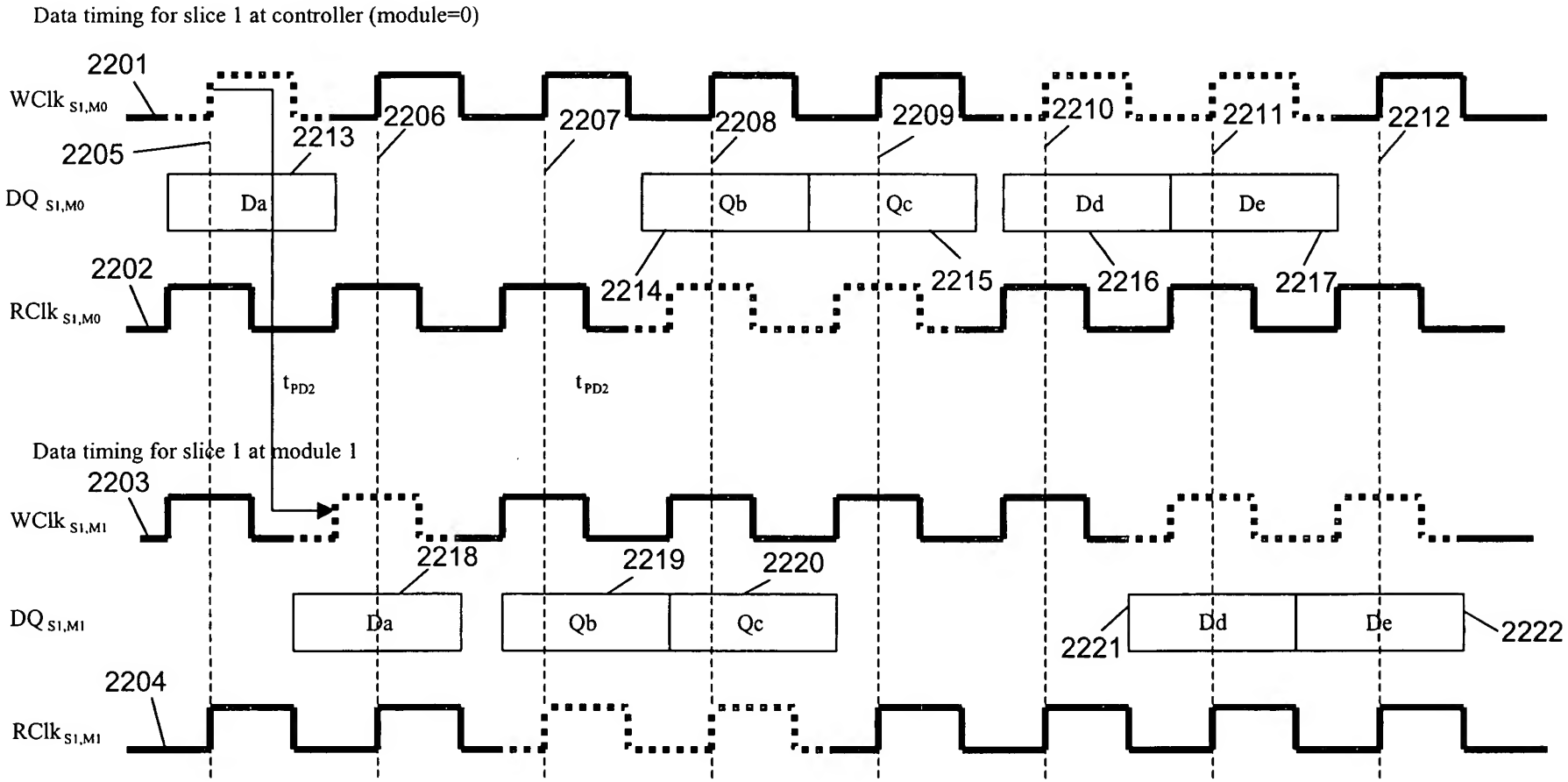


FIG. 22

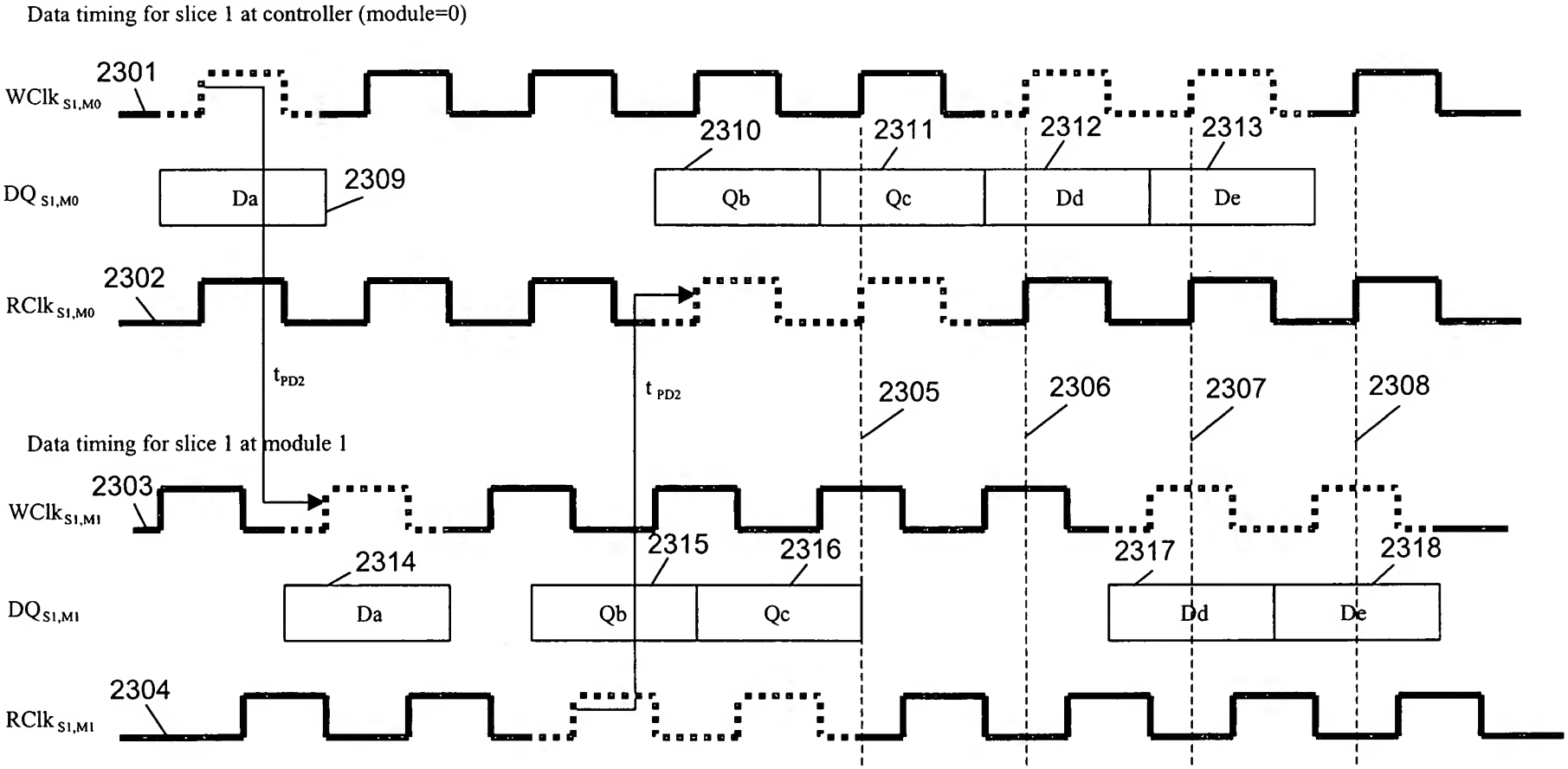


FIG. 23

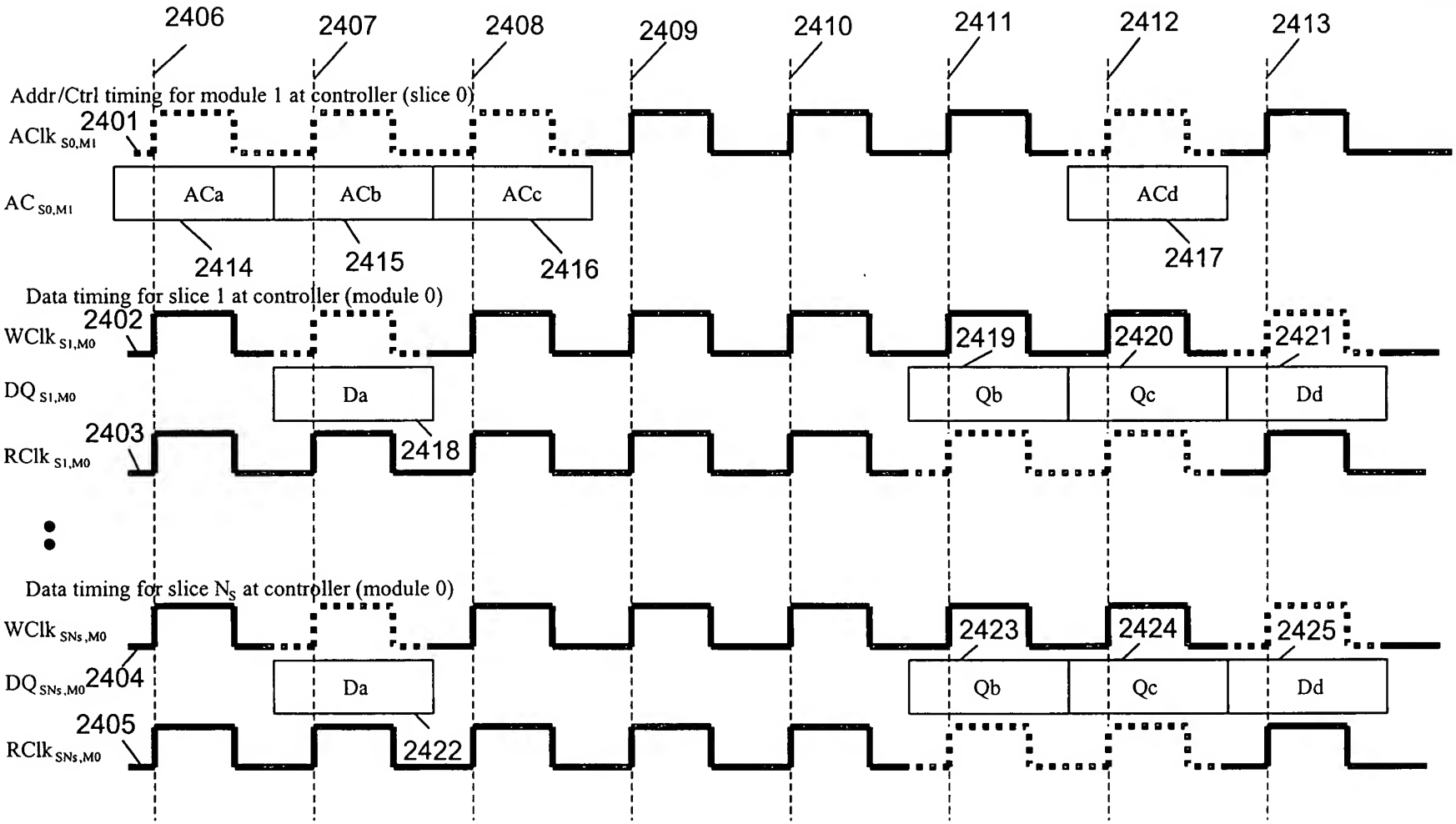


FIG. 24

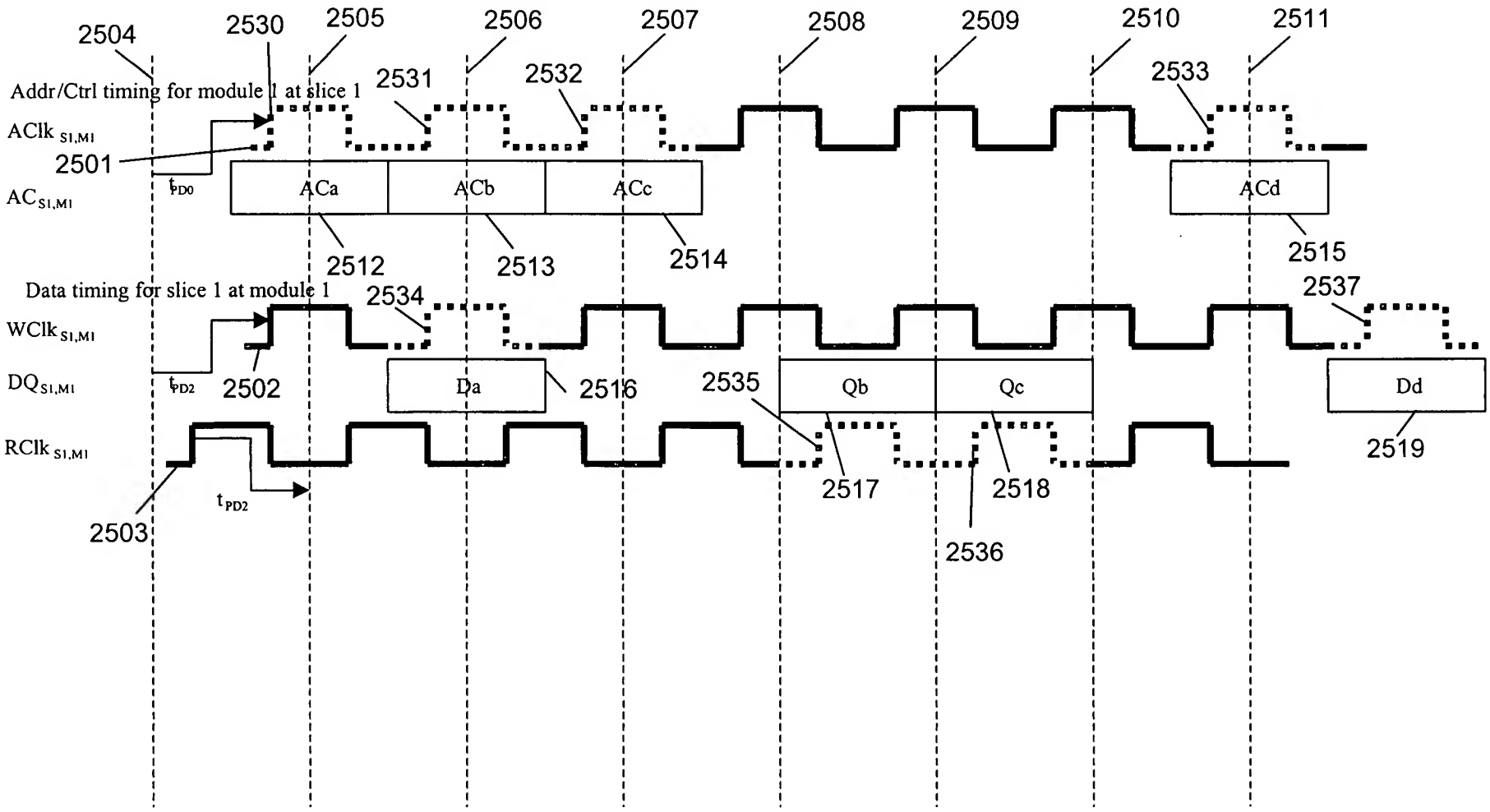


FIG. 25

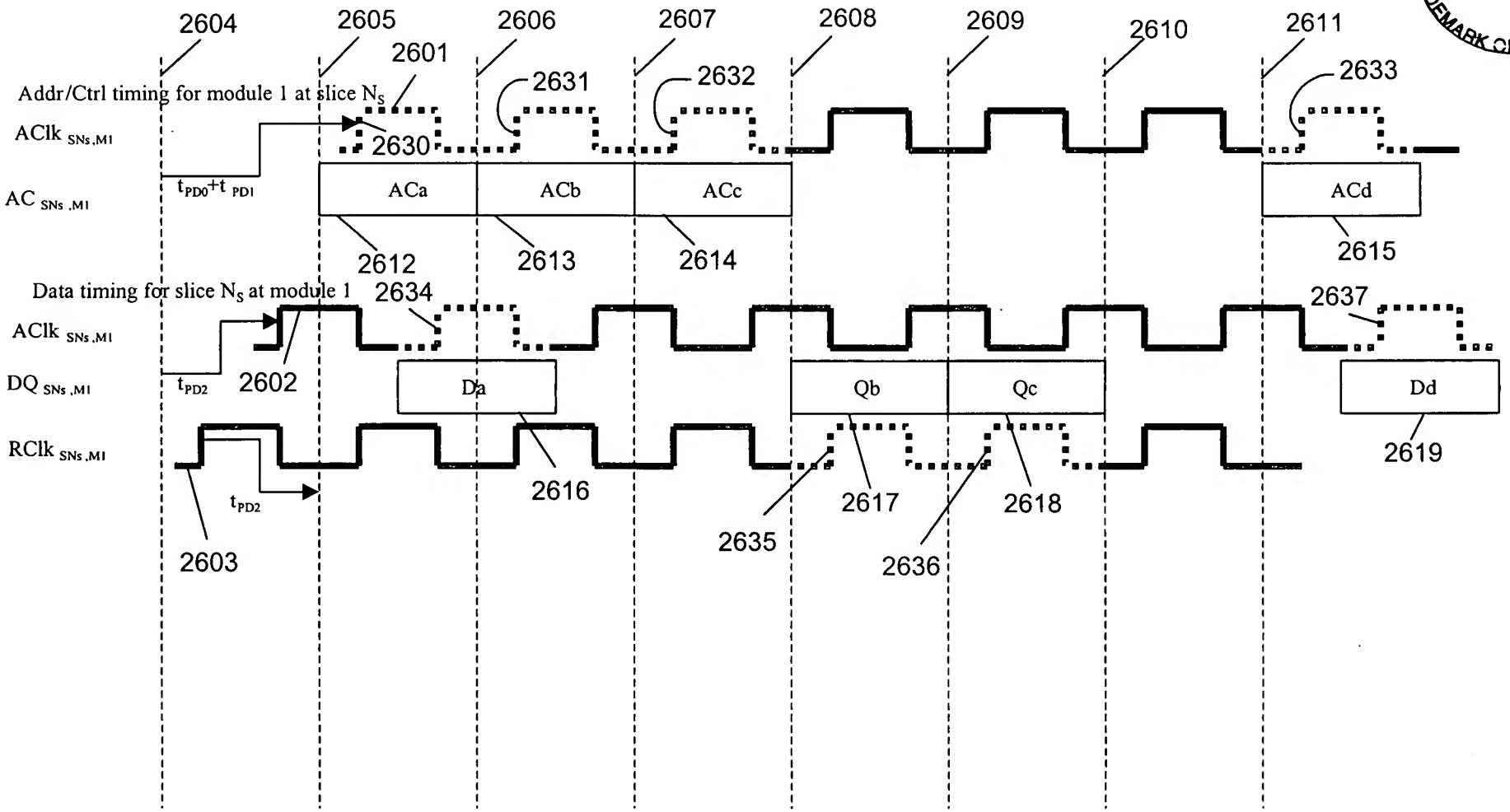


FIG. 26

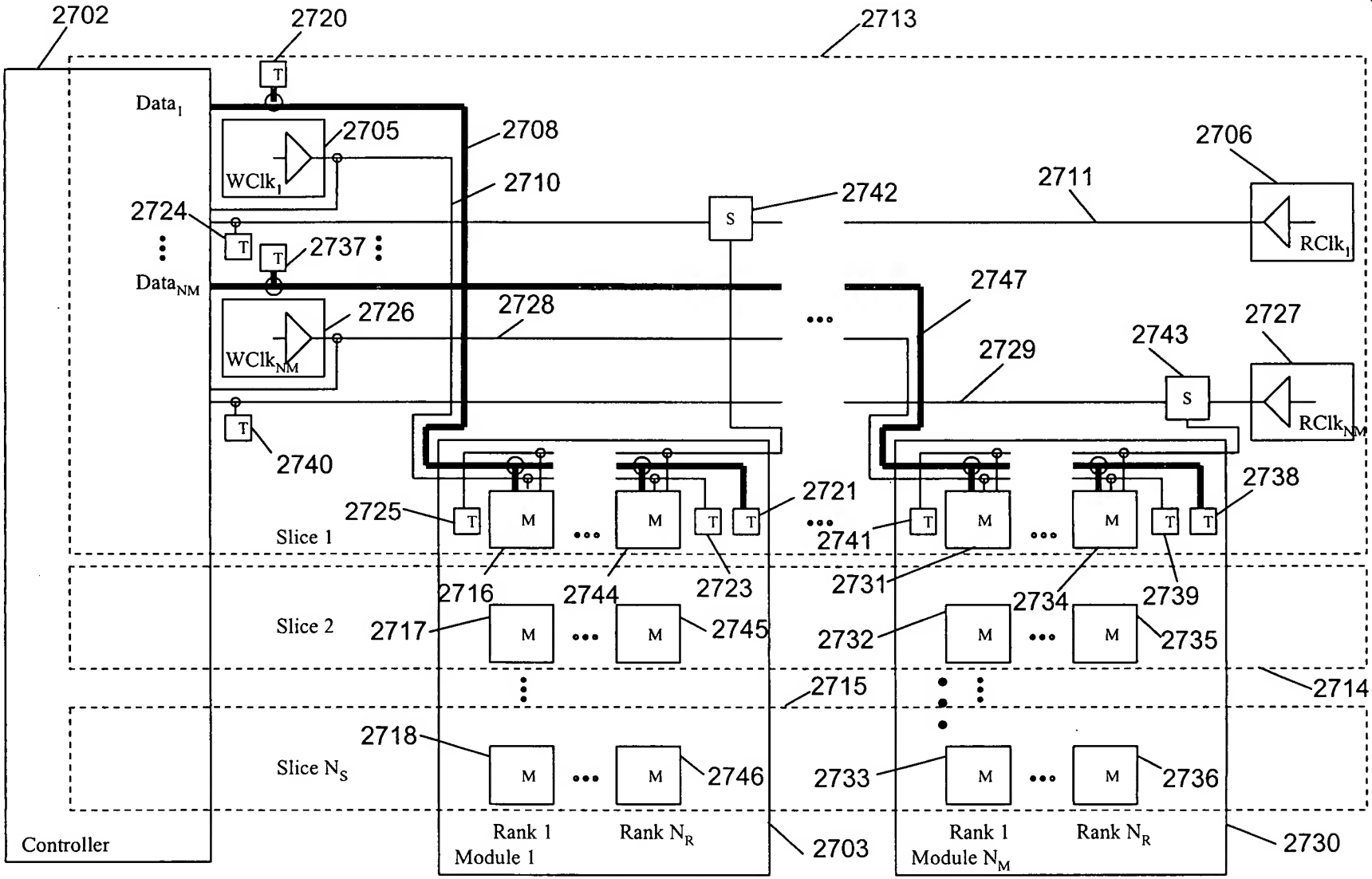


FIG. 27

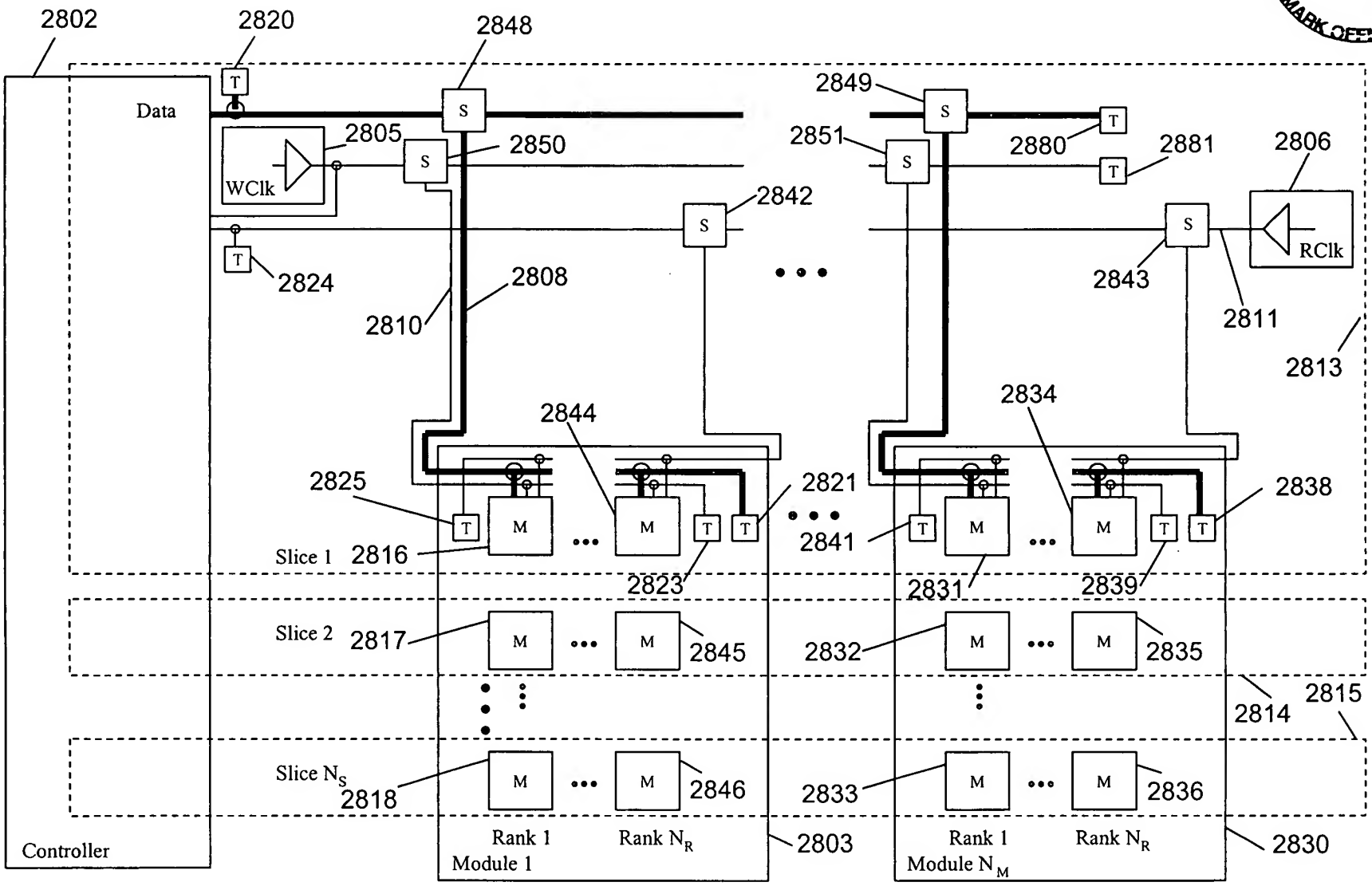


FIG. 28

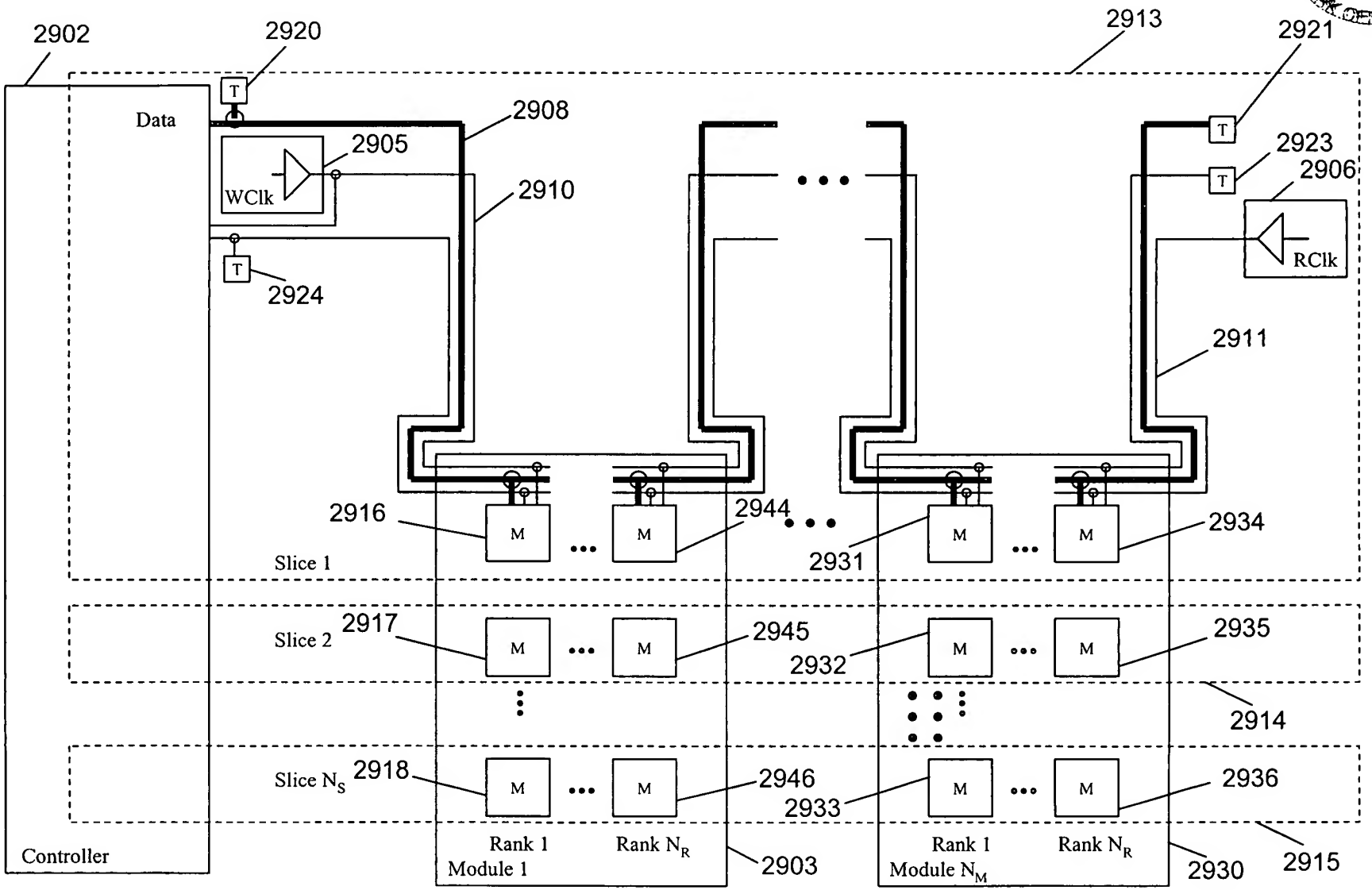


FIG. 29

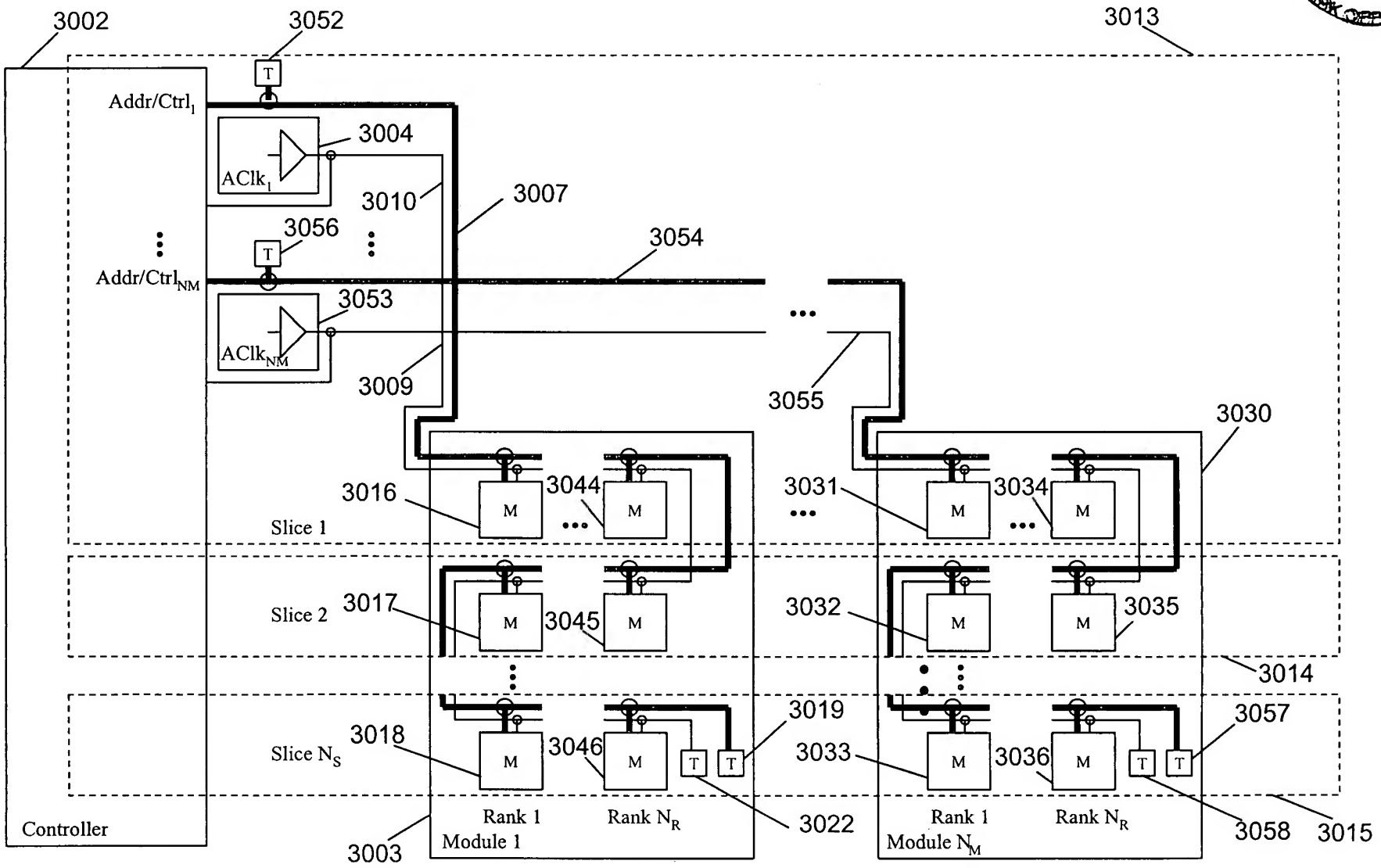


FIG. 30

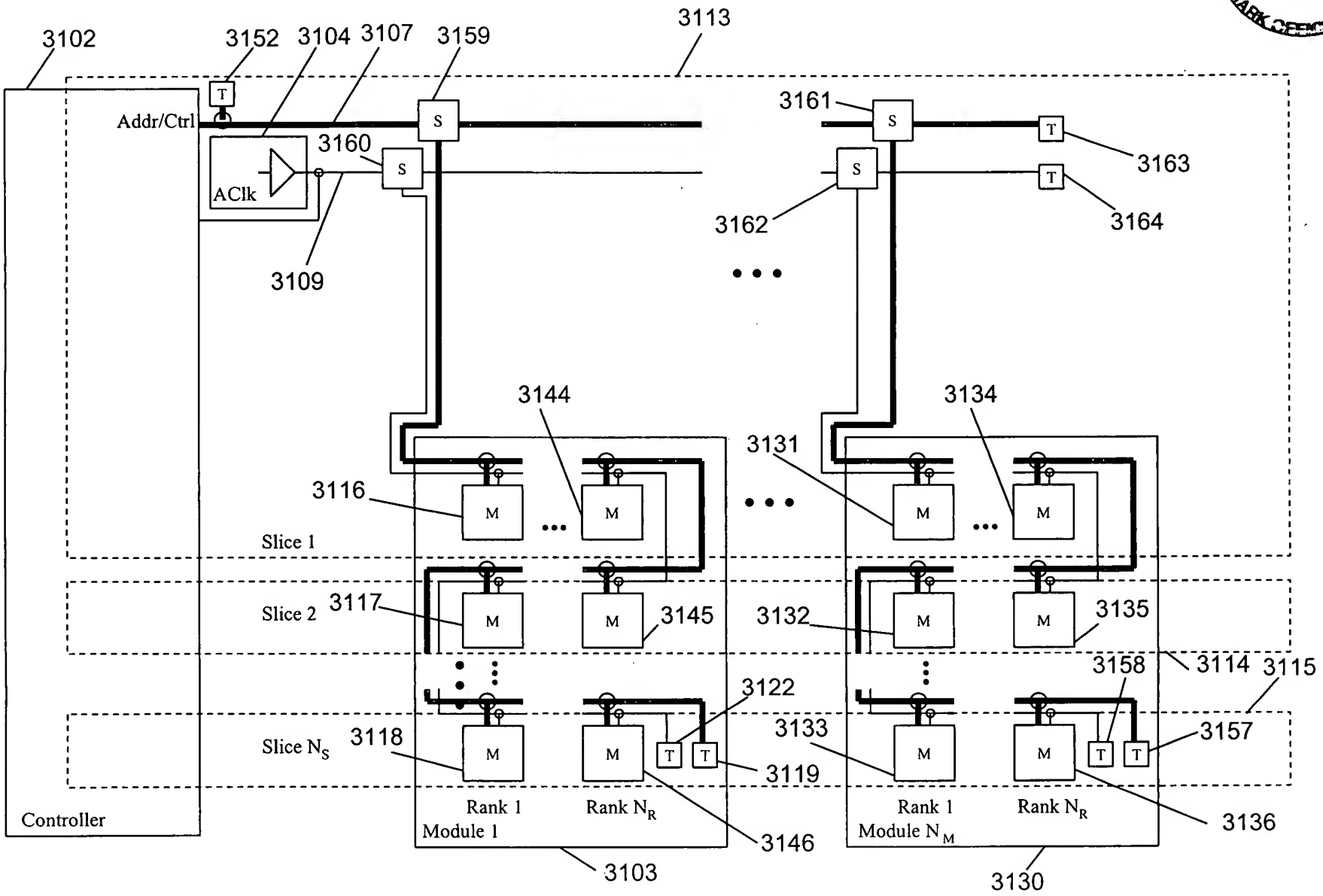


FIG. 31

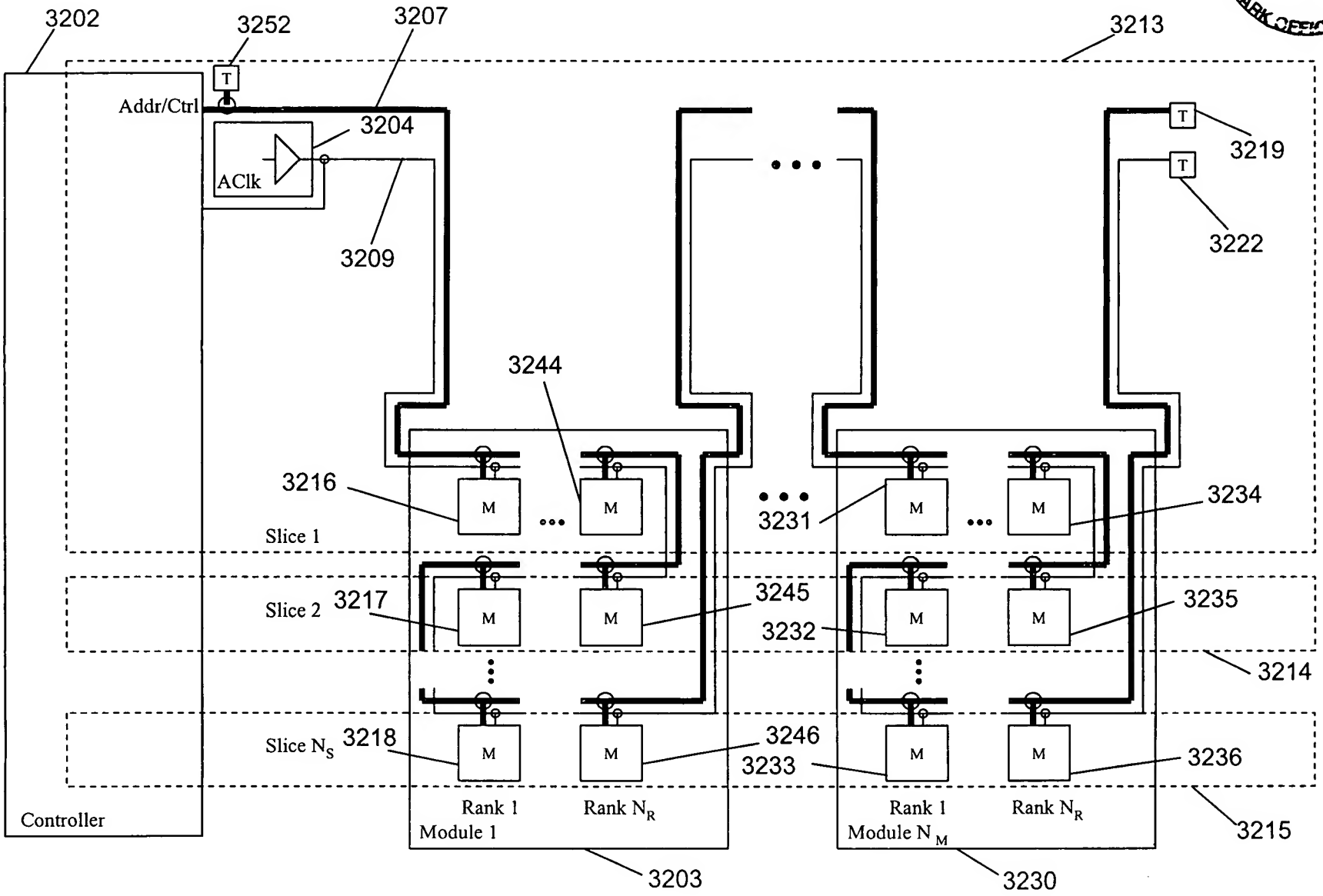


FIG. 32

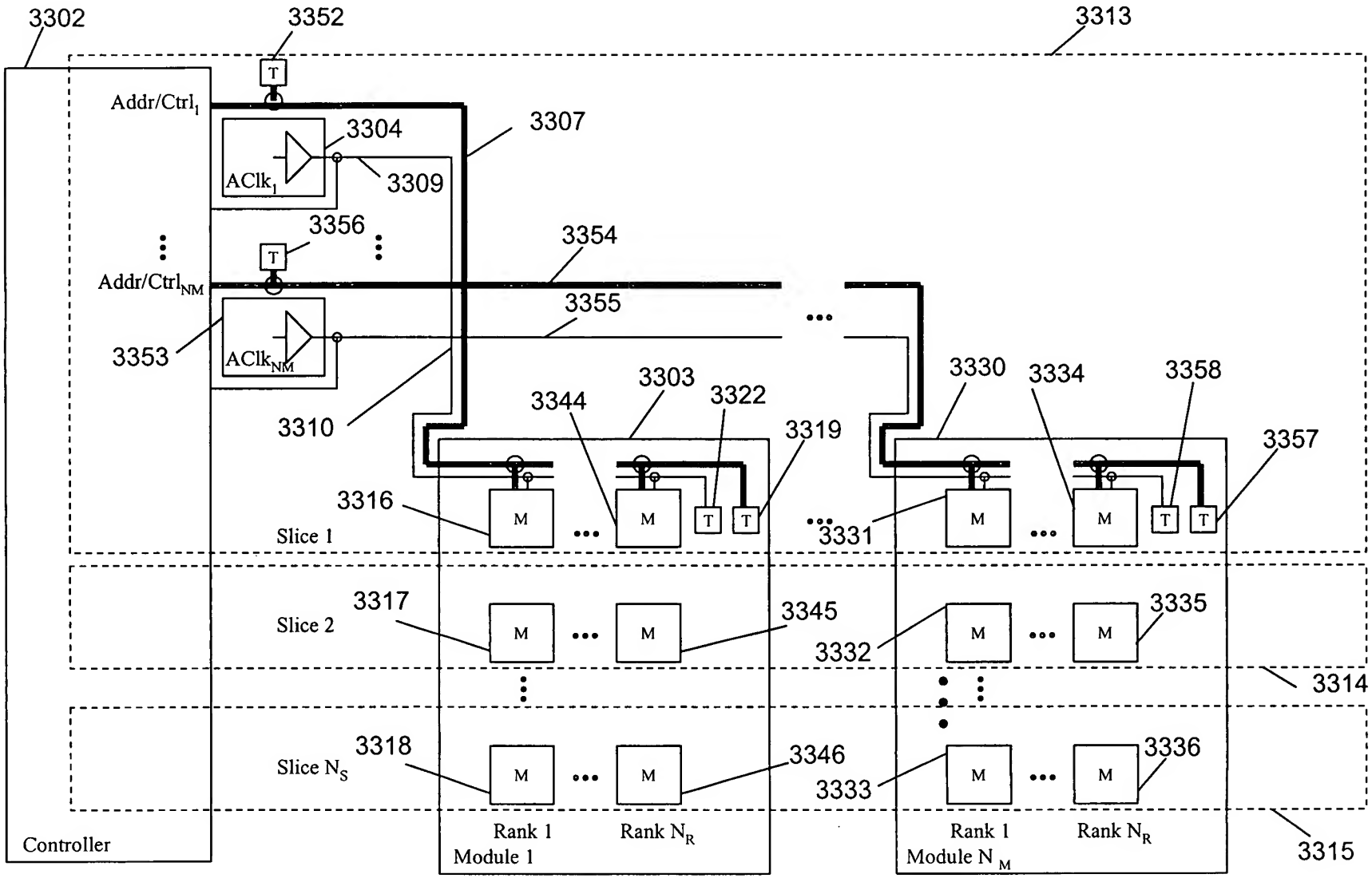


FIG. 33

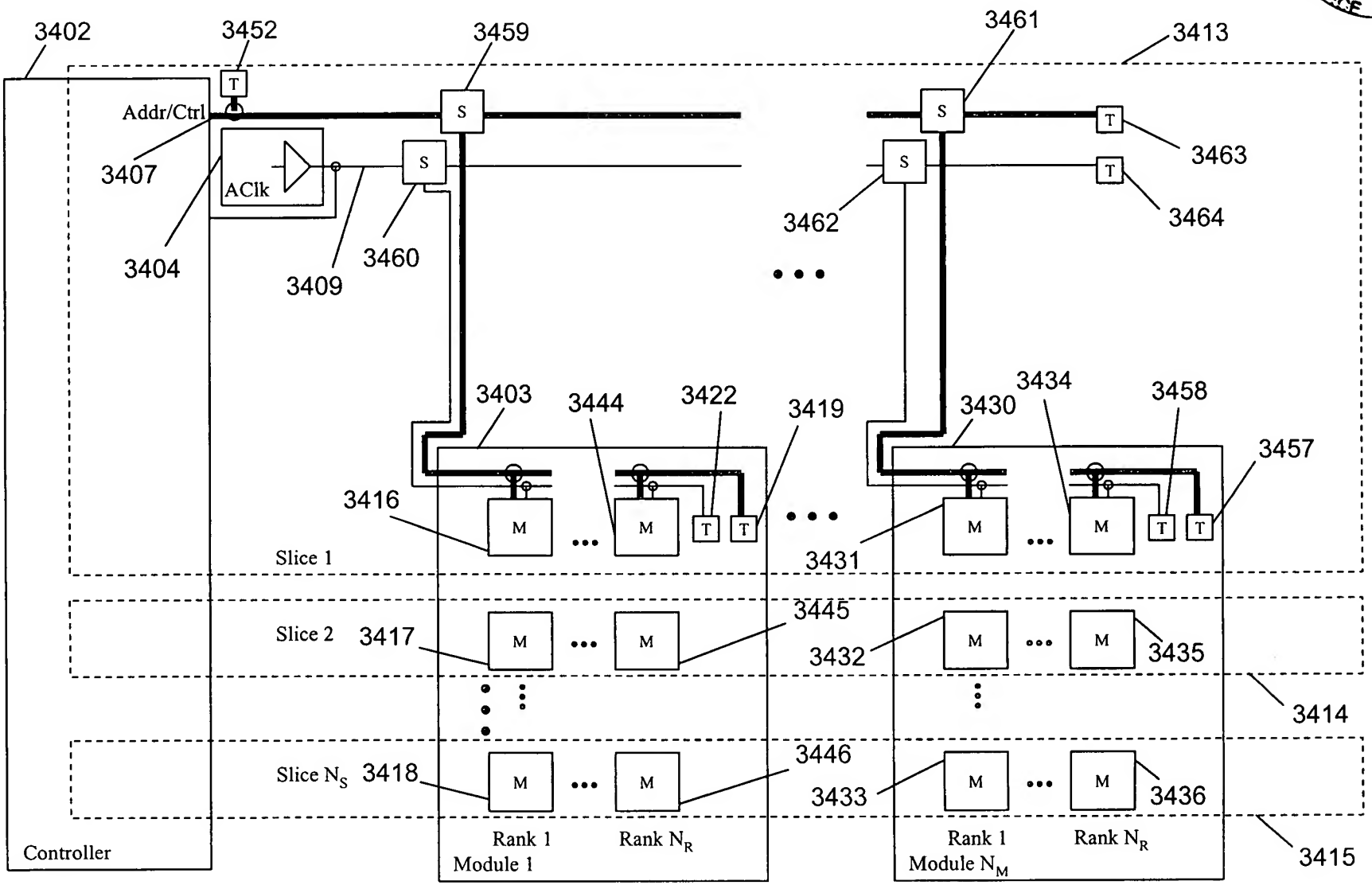


FIG. 34

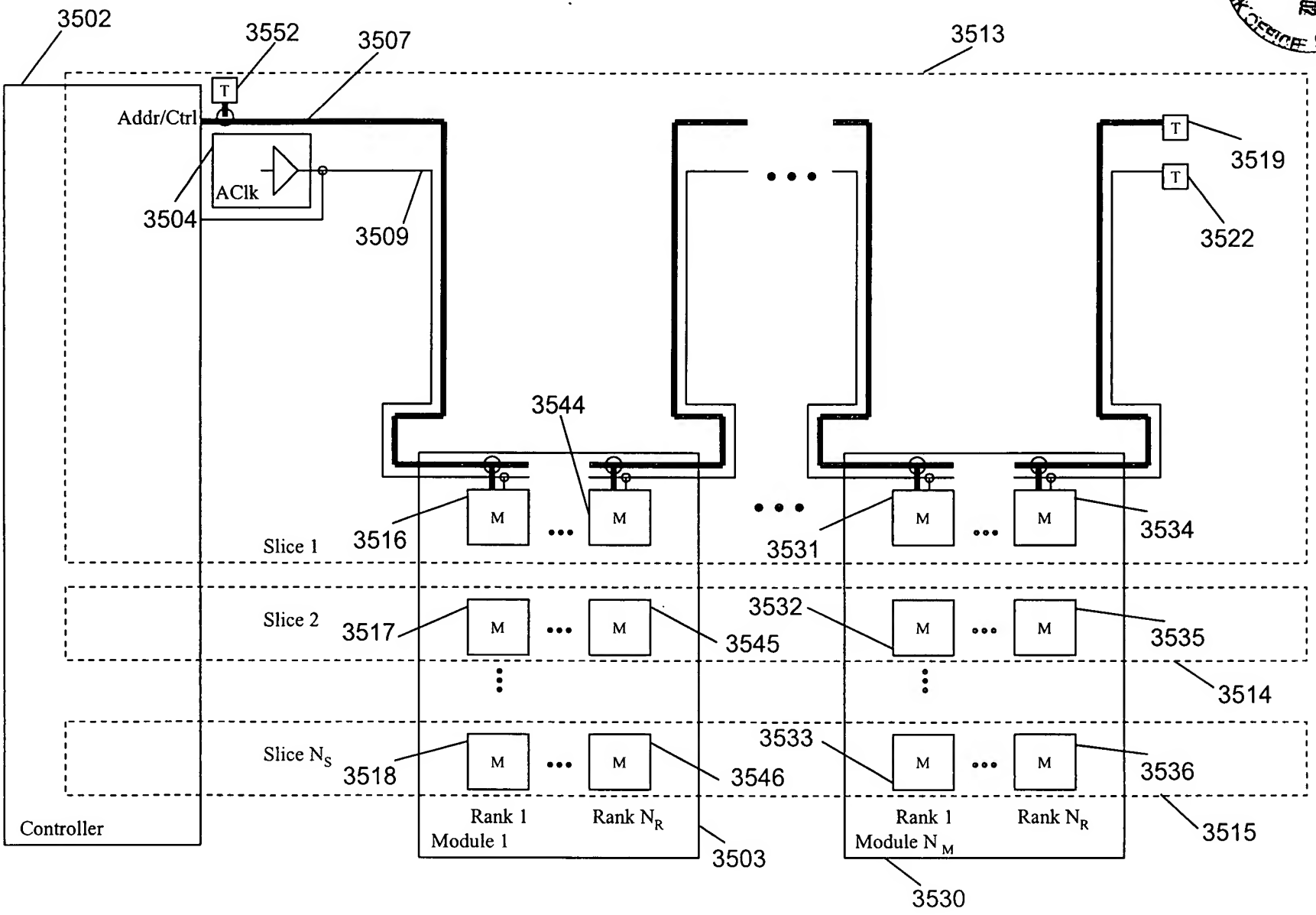


FIG. 35

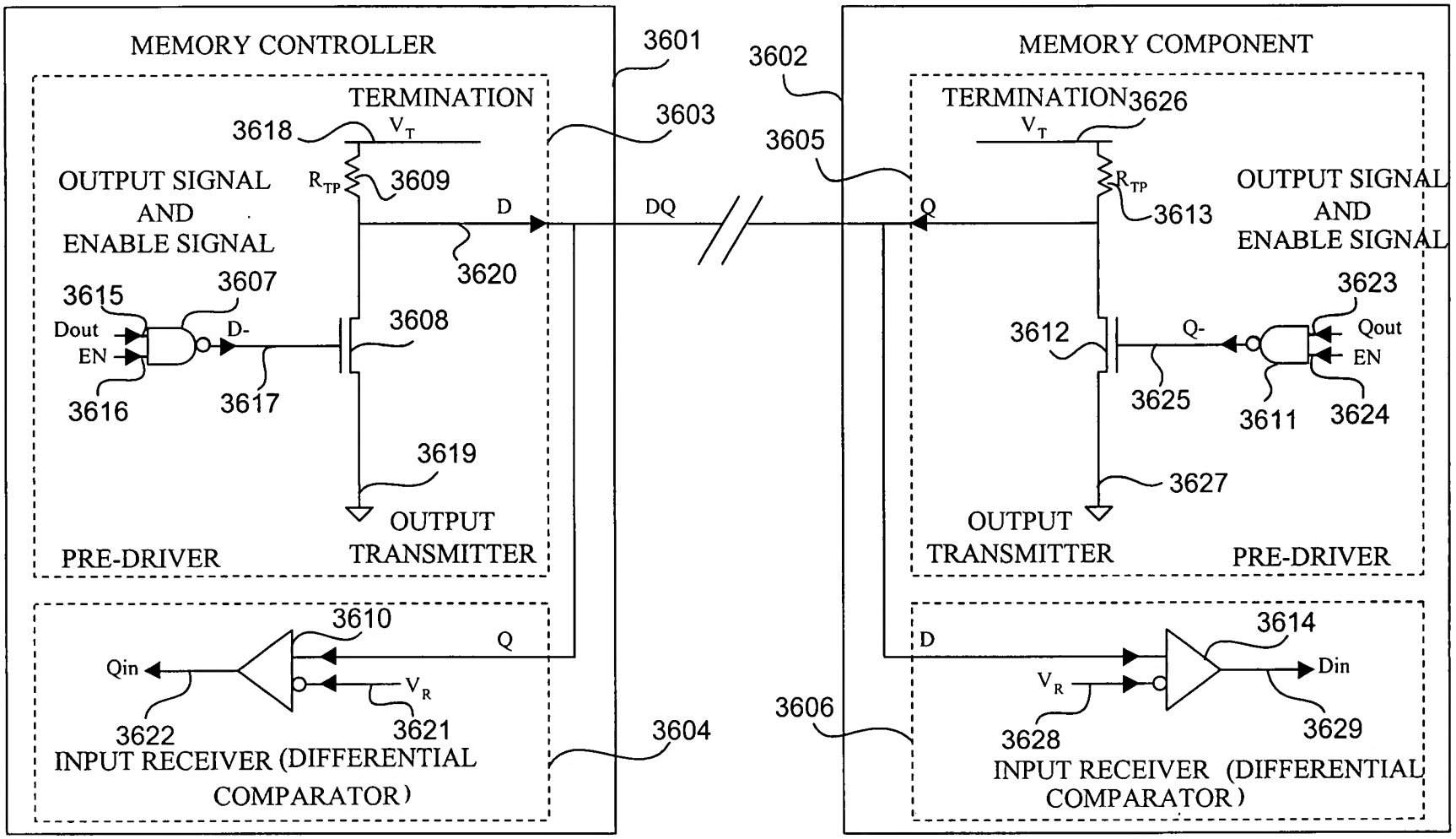


FIG. 36

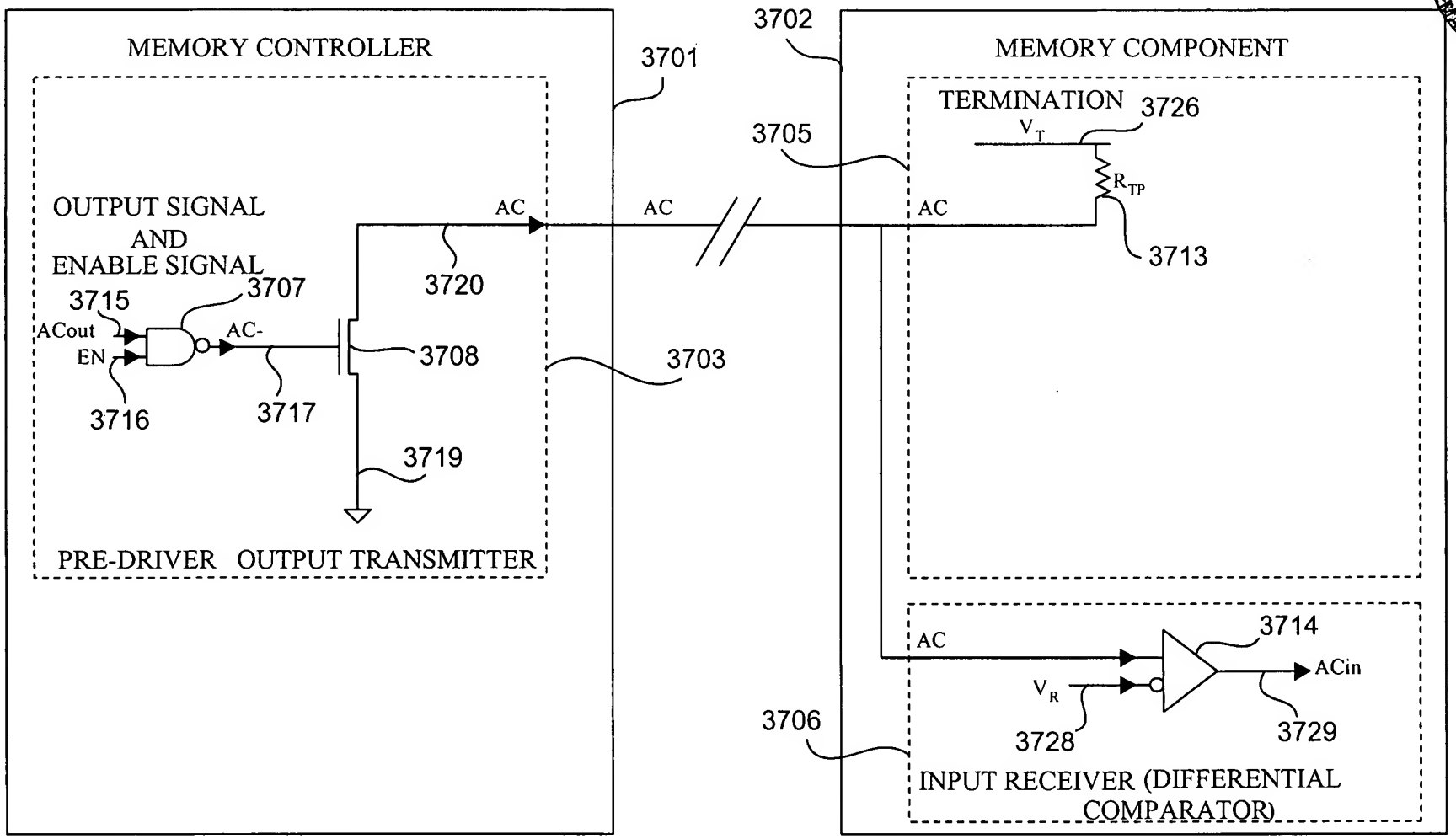

MEMORY CONTROLLER
3701
3702
MEMORY COMPONENT
TERMINATION
3726
V_T
3705
R_{TP}
OUTPUT SIGNAL
AND
ENABLE SIGNAL
AC
AC
AC
3720
3713
3715
3707
ACout
EN
AC-
3708
3703
3716
3717
3719
PRE-DRIVER OUTPUT TRANSMITTER
AC
3714
ACin
V_R
3706
3728
3729
INPUT RECEIVER (DIFFERENTIAL
COMPARATOR)

FIG. 37

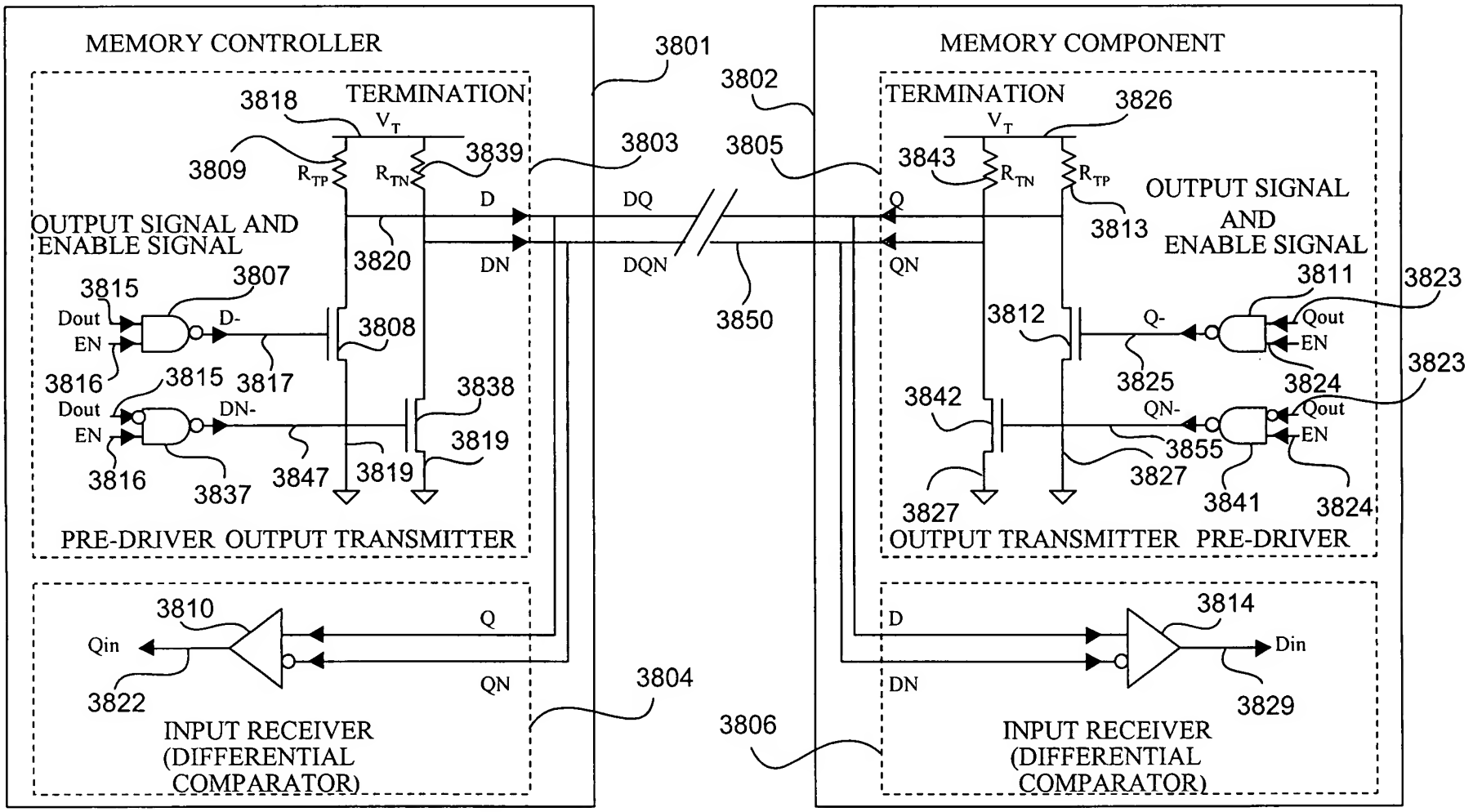


FIG. 38